

Timing Diagram

Lecture objectives: at the end of this lecture the student will able to:

- 1- Define the timing diagram.
- 2- Study and representation of the clock signal.
- 3- Determine the types of 8085 machine cycles.

9.1 Some of Definitions:

9.1.1 Timing Diagram: Timing diagram is the display of initiation of read/write and transfer of data operations under the control of 3-status signals $\overline{IO/\overline{M}}$, S_1 , and S_0 .

9.1.2 Instruction Cycle: It is *fetching, decoding* and *executing* of a single instruction, which consists of one to five read or writing operations between processor and memory or IO devices.

9.1.3 Machine Cycle: It is the one cycle that required to move one byte of data in or out of the microprocessor. Each one machine cycle consists 3 to 6 clock period, referred to as T-state.

9.1.4 T-state: It is the time of one clock period which depends on operating frequency. Another definition of the T-state is a portion of an operation carried out in one system clock period.

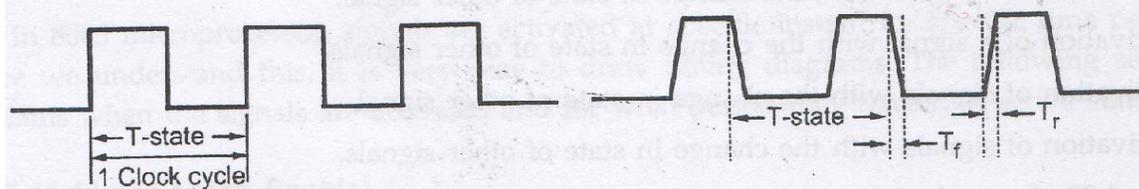
There are seven different types of machine cycles in 8085A. Table 9.1 show these types which its identified depend on status signals $\overline{IO/\overline{M}}$, S_1 , and S_0 . These signals are generated at the beginning of each machine cycle and remained valid for the duration of the cycle.

9.2 Clock Signal:

The 8085 divide the clock frequency provided by X_1 and X_2 inputs by 2 which is called operating frequency. Ideally, the clock signals should be square wave with zero rise time and fall time, but practically, cannot get zero rise time and fall time. Therefore, the clock and other signals are always shown with finite rise and fall times see Fig. 9.1.

Table 9.1: Machine cycle status and control signals.

Machine cycle	Status			Controls		
	$\overline{IO/\overline{M}}$	S_1	S_0	\overline{RD}	\overline{WR}	\overline{INTA}
Opcode Fetch (OF)	0	1	1	0	1	1
Memory Read	0	1	0	0	1	1
Memory Write	0	0	1	1	0	1
I/O Read (I/OR)	1	1	0	0	1	1
I/O Write (I/OW)	1	0	1	1	0	1
Acknowledge of INTR (INTA)	1	1	1	1	1	0
BUS Idle (BI) : DAD	0	1	0	1	1	1



(a) (b)
Figure 9.1: Clock signal representation; a)ideal, b) Practical

9.2.1 Single and group of signals:

Single signal is represented by a line. It may have status either logic 0 or logic 1 or tri-state as in Fig. 9.2. While, group of signals is also called a bus e.g. address bus and data bus. To avoid complications in the timing diagram these signal are grouped and shown in the form of block as shown in Fig. 9.3.

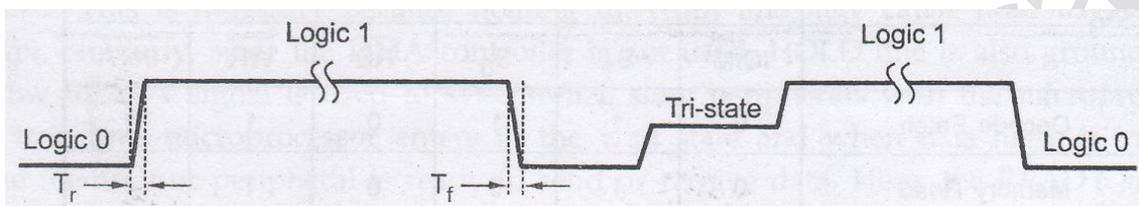


Figure 9.2: Single signal representation.

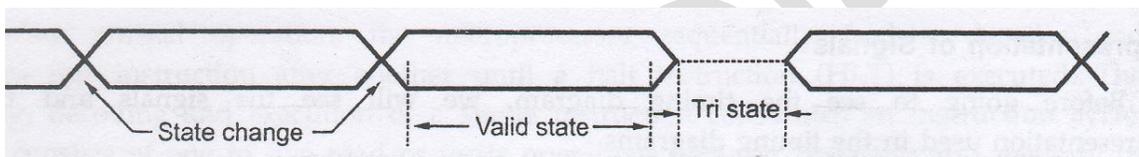


Figure 9.3: Group of signals representation.

9.2.2 Signal Timing:

In 8085 microprocessor, signals are activated at specific instant for specific time period. Once we understand this, it is very easy to draw timing diagram. Examples below explain ALE signals activation and what period they remain in active state.

Ex.1/ALE is active high signal. It is activated in the beginning of T₁ state of machine cycle, except bus idle machine cycle, and it remain active in T₁ state only as shown in Fig. 9.4

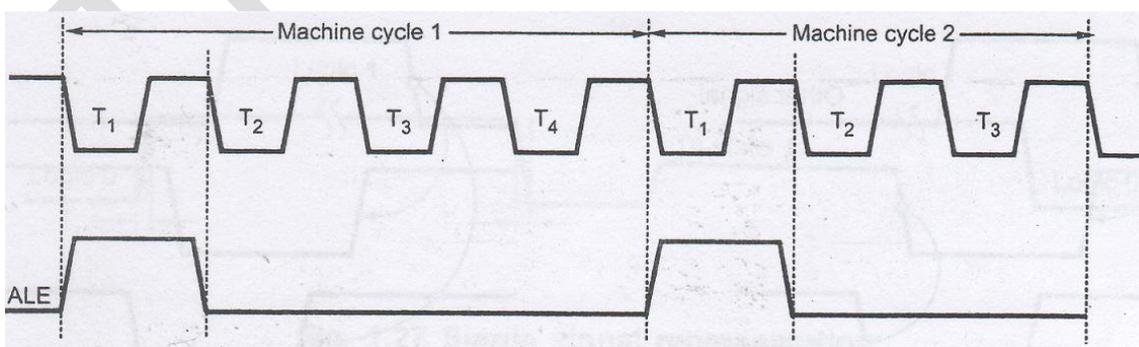


Figure 9.4: ALE activation and its period.

Ex.2/ A_0-A_7 (Lower Byte Address) is available on the multiplexed address/data bus (AD_0-AD_7) during T_1 state of machine cycle, except bus idle machine cycle as shown in Fig. 9.5. below:

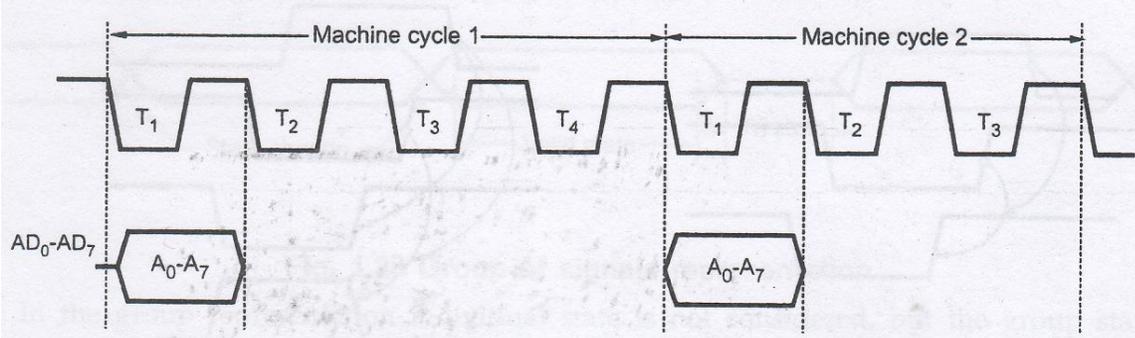


Figure 9.5: Lower address on the multiplexed bus.

Ex.3/ D_0-D_7 (Data Bus) it used to transfer the data from IO devices or memory to microprocessor or from microprocessor to IO device or memory during T_2 and T_3 states. It is important to note that through reading data operation, the data will appear on the data bus during the later part of the T_2 state. while, in writing data operation the data will appear on data bus at the beginning of T_2 state, see Fig. (9.6 a & b).

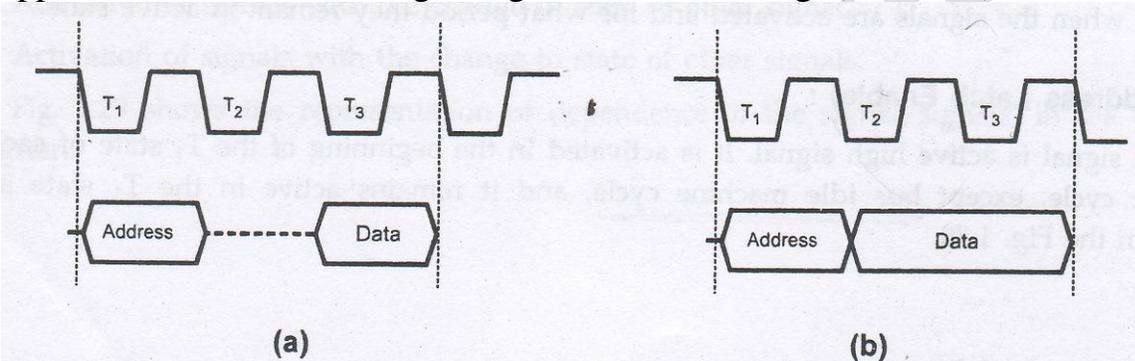


Figure 9.6: Data bus status; a) through reading operation, b) through writing operation.

Why there are difference in appearing of data on data bus through reading and writing operation.

Ex.4/ A_8-A_{15} (Higher Byte Address) is available on the address bus during T_1 , T_2 , and T_3 states of each machine cycle, except bus idle machine cycle s shown in Fig. 9.7. below:

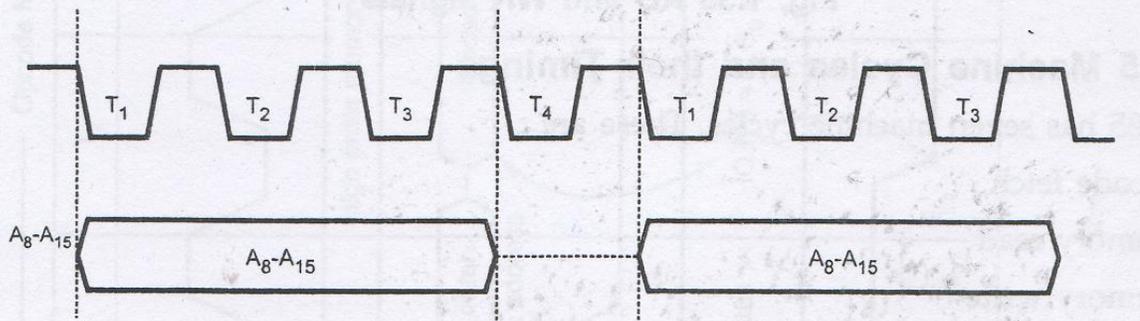


Figure 9.7: Higher byte address status.

Ex.5/ $\overline{IO/\overline{M}}$, S_1 , S_2 signals are called status signals. They determine the type of machine cycle to be executed. They are activated at beginning of T_1 -state of each machine cycle and remain active till the end of the machine cycle as shown in Fig. 9.8.

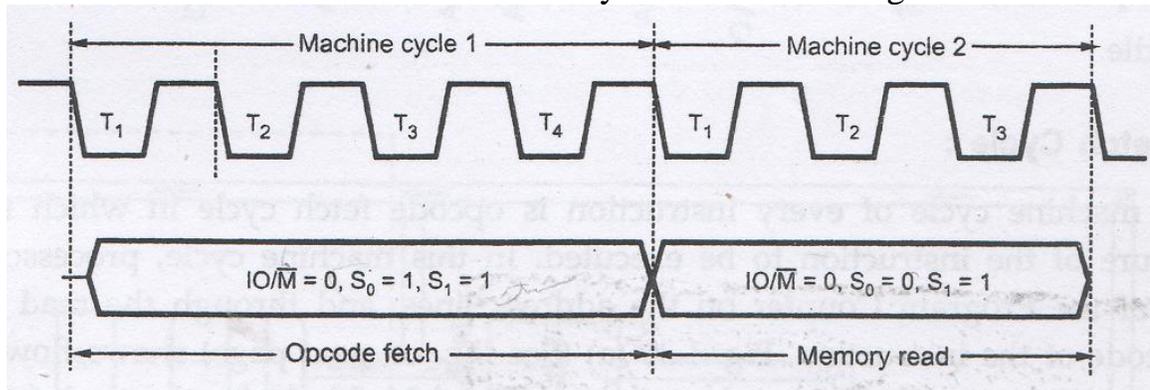


Figure 9.8: Status signals timing diagram.

Ex.6/ \overline{RD} and \overline{WR} determine the direction of data flow between microprocessor and IO devices or memory locations. As we noted that these signals are activated through T_2 & T_3 states of machine cycle. Both signals are never active at a time. The Fig. 9.9 shows the timing diagram of \overline{RD} and \overline{WR} signals.

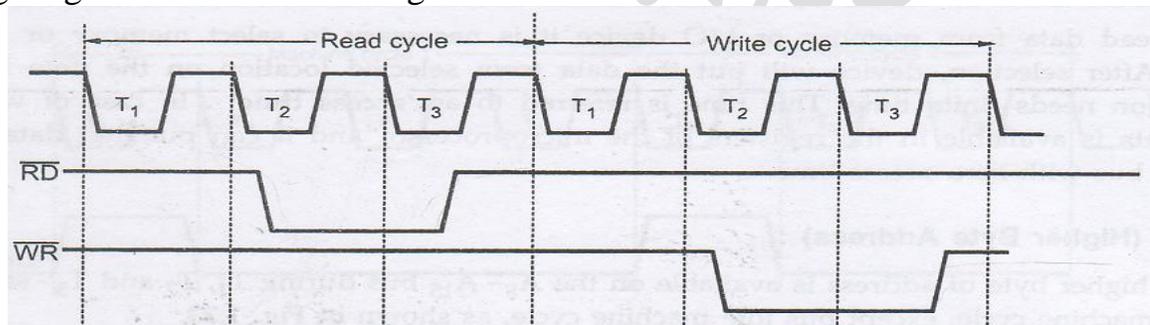


Figure 9.9: Read and write signals timing diagram.

9.3 8085 Machine Cycles and their Timings:

The 8085 has seven machine cycles. These are:

1. Opcode fetch.
2. Memory read.
3. Memory write.
4. I/O read.
5. I/O write.
6. Interrupt acknowledge.
7. Bus idle.

9.3.1 Opcode Fetch Cycle:

The first machine cycle of every instruction is opcode fetch cycle in which the 8085 finds the nature of the instruction to be executed. In this machine cycle, the microprocessor places the contents of PC on the address bus then by reading operation it reads the opcod of an instruction from determined memory location. The length of this cycle is not fixed. Steps below explain opcode fetch cycle in

more details. Figure 9.10 shows the timing diagram and data flow of opcode fetch cycle.

- **Step1: (T₁ state)** The 8085 processor places the contents of program counter on the address bus, activate the ALE and send the status signals $\overline{IO/\overline{M}}$, S₁, and S₀ with logical status (0 1 1) respectively.
- **Step 2: (T₂ state)** The low order address disappears from AD₀-AD₇ lines. Also, 8085 processor activates the \overline{RD} signals to enable the addressed memory location which places its contents on the data bus (AD₀-AD₇).
- **Step 3: (T₃ state)** The processor loads the contents of data bus on its Instruction Register and deactivates the \overline{RD} signal to disables the memory devices.
- **Step4: (T₄ state)** the processor decode the opcode, and on the basis of the instruction received, it decides whether to enter T₅ or to enter T₁ of new machine cycle. One byte instructions those operate on eight bit data (8 bit operand) are executed in T₄. for example: MOV C,B- ANA E- ADD B- INR C- RAR ...etc.
- **Step5: (T₅ & T₆ states)** the processor performs stack write, internal 16 bits, or conditional return operations depending upon the type of instruction. One byte instructions those operate on 16 bit data are executed in T₅ & T₆. For example DCX H, PCHL, SPHL, INX H, etc.

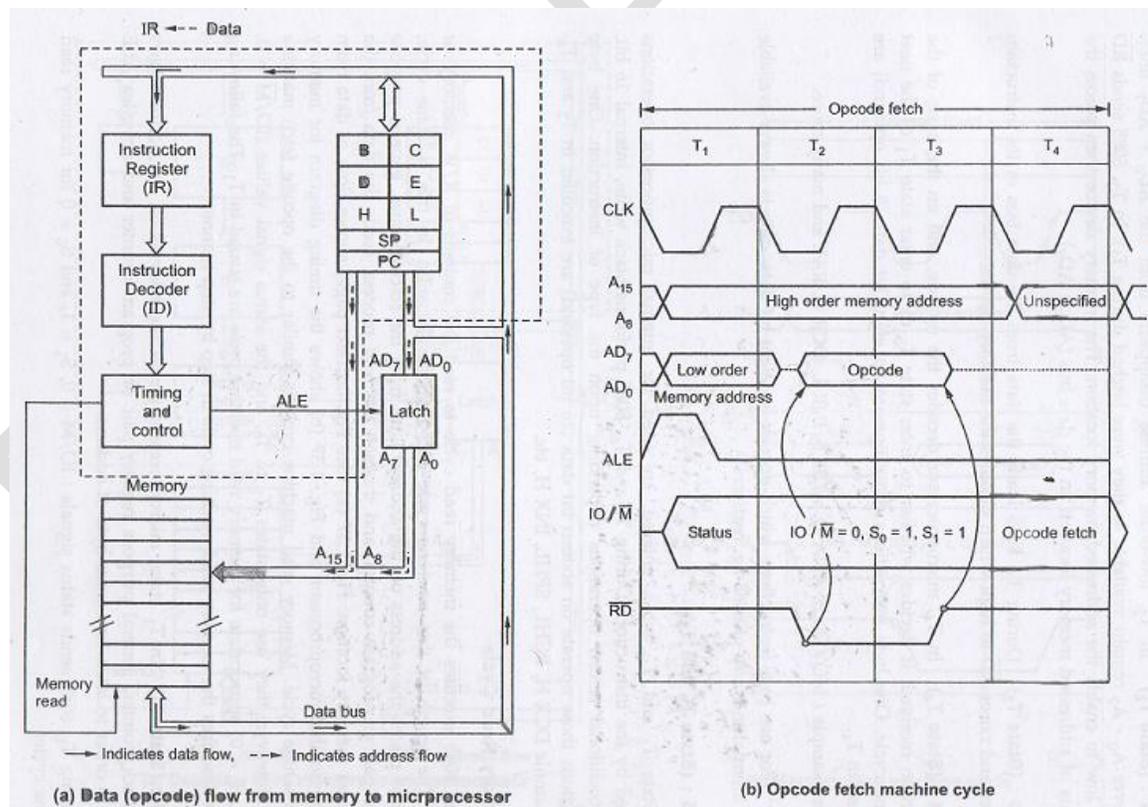


Figure 9.10: details of opcode machine cycle.

9.3.2 Memory read cycle:

The microprocessor executes the memory read cycle to read the data from RAM or ROM memory. 8085 processor executes this machine cycle in 3 T-states. Steps below show the details of this machine cycle:

- **Step1 (T₁ state):** processor places the address on the address lines from SP, Rp, or PC and activates ALE in order to latch low-order of address. Also, it sends the status signals with logical status (0 1 0) for memory read machine cycle.
- **Step2 (T₂ state):** , 8085 processor activates the \overline{RD} signals to enable the addressed memory location which places its contents on the data bus (AD₀-AD₇).
- **Step 3: (T₃ state)** The processor loads the contents of data bus on specified register (F, A, B, C, D, E, H, and L) and deactivates the \overline{RD} signal to disables the memory devices.

Figure 9.11 shows the timing diagram and data follow for read memory machine cycle.

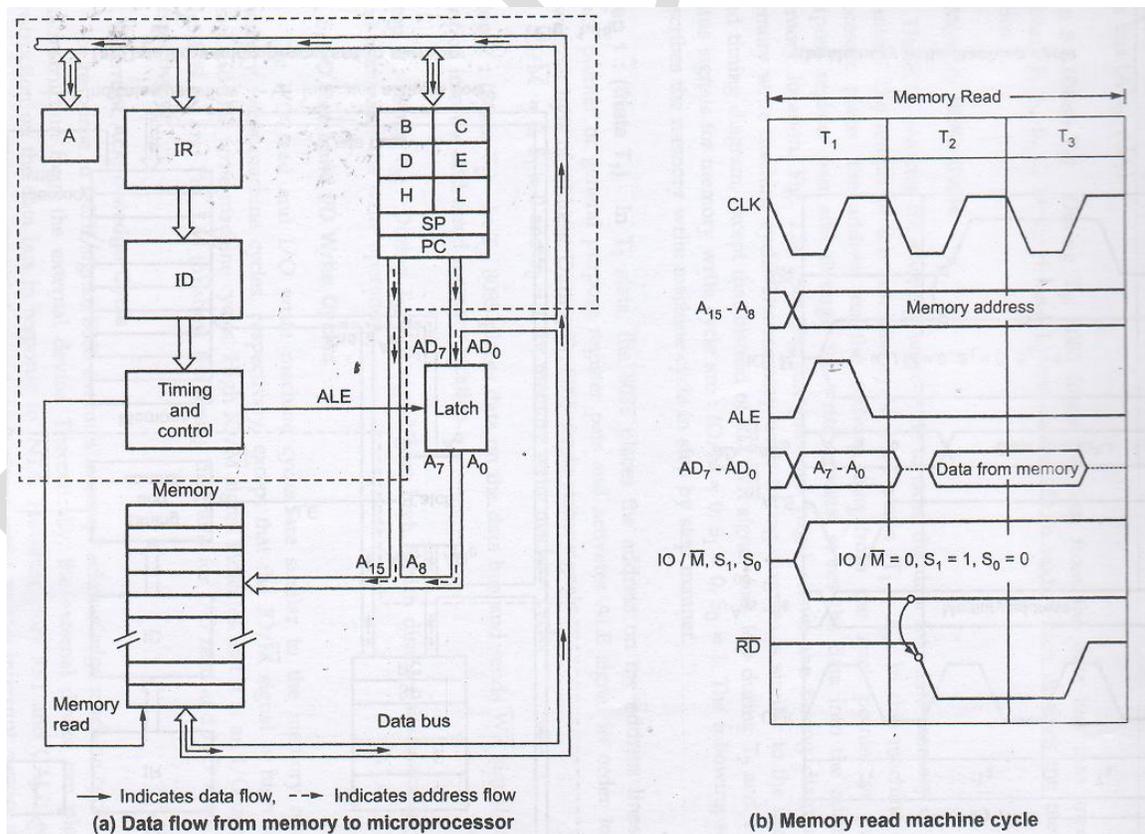


Figure 9.11: details of memory read machine cycle.

9.3.3 Memory write cycle:

The microprocessor executes the memory write cycle to store the data into RAM or stack memory. 8085 processor executes this machine cycle in 3 T-states. Steps below show the details of this machine cycle:

- **Step1 (T₁ state):** processor places the address on the address lines from SP or Rp and activates ALE in order to latch low-order of address. Also, it sends the status signals with logical status (0 0 1) for memory write machine cycle.
- **Step2 (T₂ state):** , 8085 processor places the data on data bus and activates the \overline{WR} signal to writing data into addressed memory location.
- **Step 3: (T₃ state)** The processor deactivates the \overline{WR} signal which disables the memory device and terminates the write operation.

Figure 9.12 shows the timing diagram and data flow for memory write machine cycle.

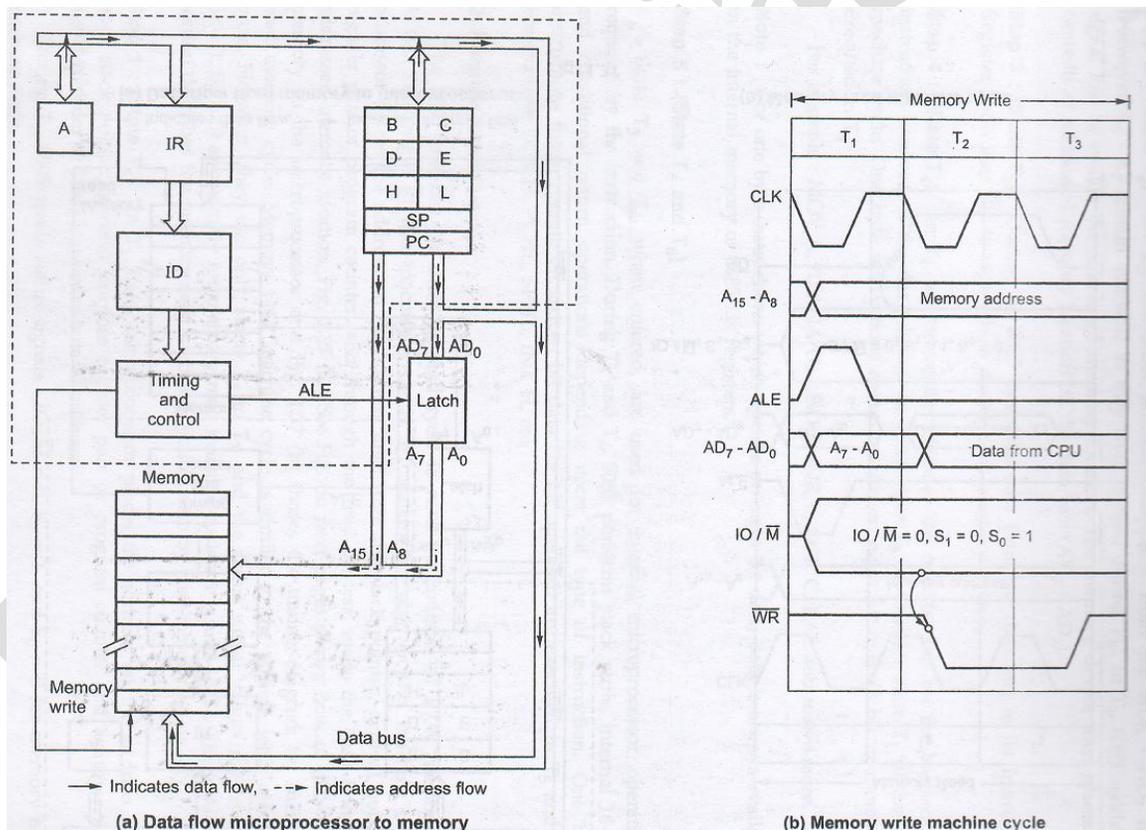


Figure 9.12: details of memory write machine cycle.

9.3.4 IO read cycle:

The microprocessor executes the IO read cycle to read the data from input device. 8085 processor executes this machine cycle in 3 T-states. Steps below show the details of this machine cycle:

- **Step1 (T₁ state):** processor places the address on the address lines from SP, Rp, or PC and activates ALE in order to latch low-order of address. Also, it sends the status signals with logical status (1 1 0) for IO read machine cycle.
- **Step2 (T₂ state):** , 8085 processor activates the \overline{RD} signals to enable the addressed input device which places its contents on the data bus (AD₀-AD₇).
- **Step 3: (T₃ state)** The processor loads the contents of data bus on specified register (F, A, B, C, D, E, H, and L) and deactivates the \overline{RD} signal to disables the input device.

Figure 9.13 shows the timing diagram and data follow for IO read machine cycle.

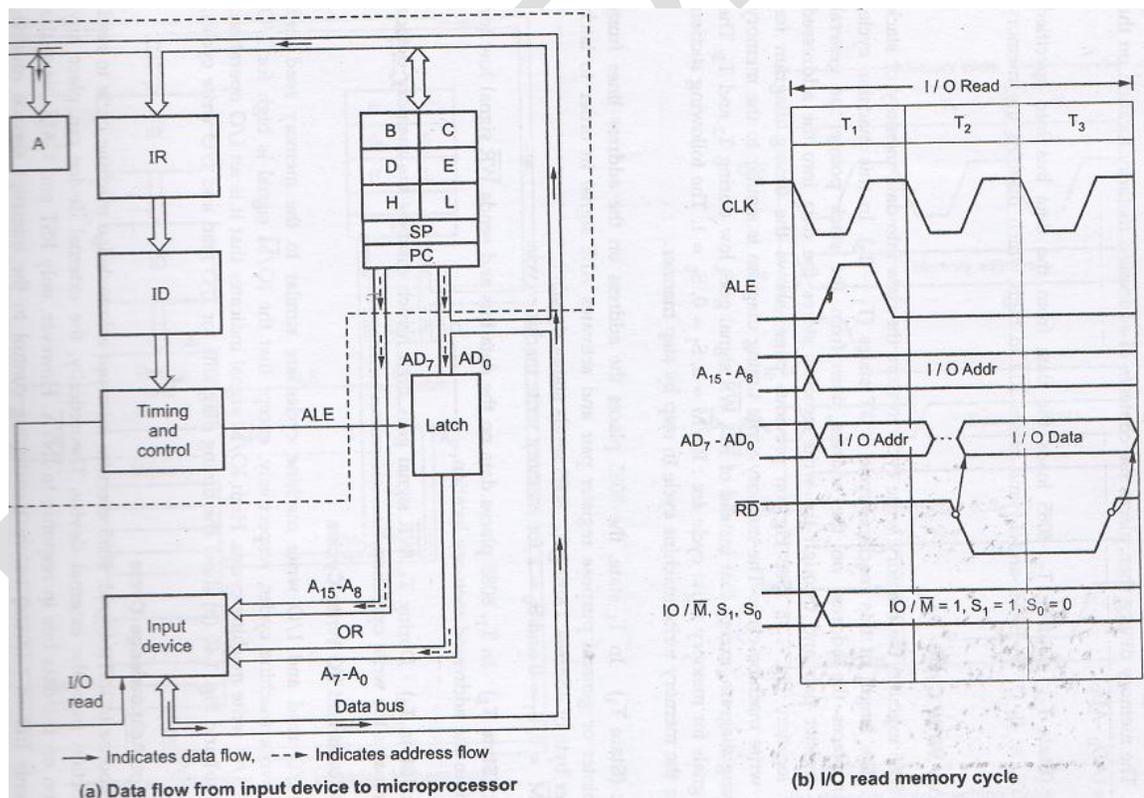


Figure 9.13: details of IO read machine cycle.

9.3.5 IO write cycle:

The microprocessor executes the IO write cycle to store the data into output device. 8085 processor executes this machine cycle in 3 T-states. Steps below show the details of this machine cycle:

- **Step1 (T₁ state):** processor places the address on the address lines from SP or Rp and activates ALE in order to latch low-order of address. Also, it sends the status signals with logical status (1 0 1) for IO write machine cycle.
- **Step2 (T₂ state):** , 8085 processor places the data on data bus and activates the \overline{WR} signal to writing data into addressed output device.
- **Step 3: (T₃ state)** The processor deactivates the \overline{WR} signal which disables the output device and terminates the writing operation.

Figure 9.14 shows the timing diagram and data follow for IO write machine cycle.

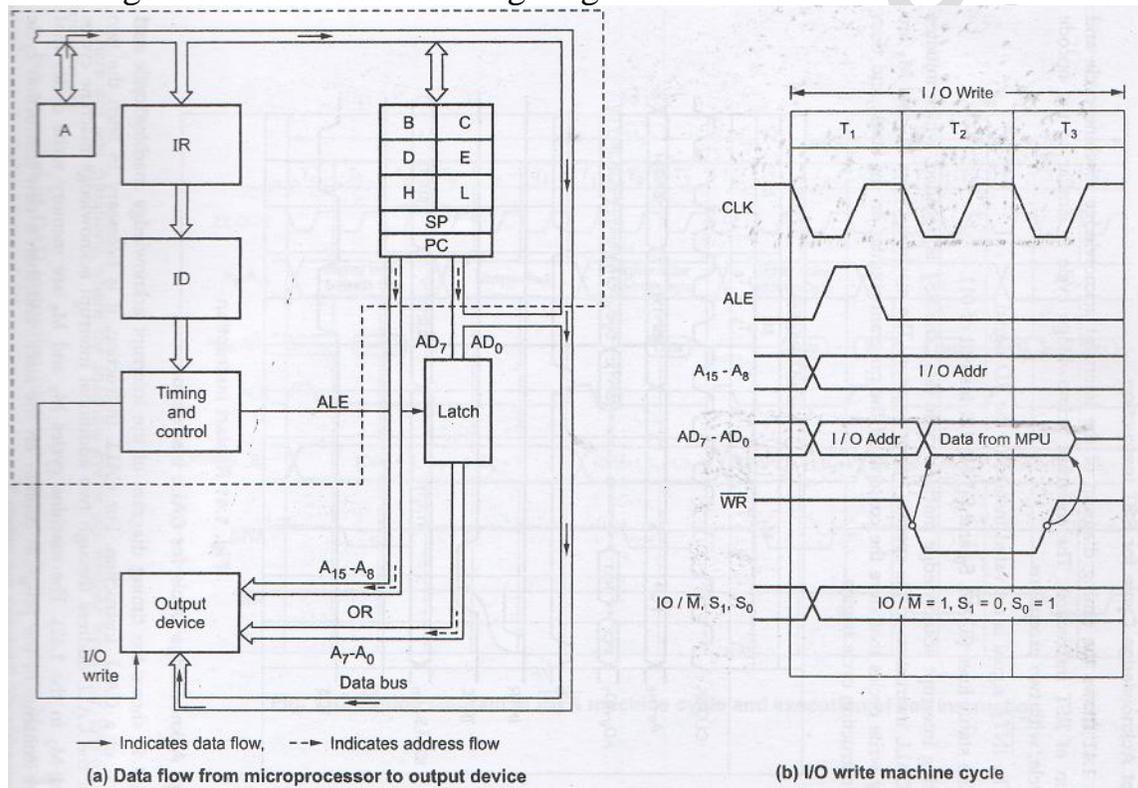


Figure 9.14: details of IO write machine cycle.

9.3.6 Interrupt Acknowledge Machine Cycle:

In response to INTR signal, processor execute interrupt acknowledge machine cycle to read an instruction from the external device. Sections below explain the machine cycle of RST and CALL instructions.

- ❖ Interrupt Acknowledge cycle for RST Instruction: The interrupt acknowledge cycle is similar to opcode fetch cycle except:
 1. The $\overline{\text{INTA}}$ signal is activated instead of $\overline{\text{RD}}$ signal.
 2. The status lines ($\text{IO}/\overline{\text{M}}, \text{S}_0$ and S_1) are 111 instead of 011.

During interrupt acknowledge machine cycle (M_1), the RST is decoded, which initiates 1 byte CALL instruction to the specific vector location. The machine cycle M_2 and M_3 are memory write cycle that store the contents of program counter on the stack, and then a new instruction cycle begins. Figure 9.15 shows the timing diagram of Restart instruction.

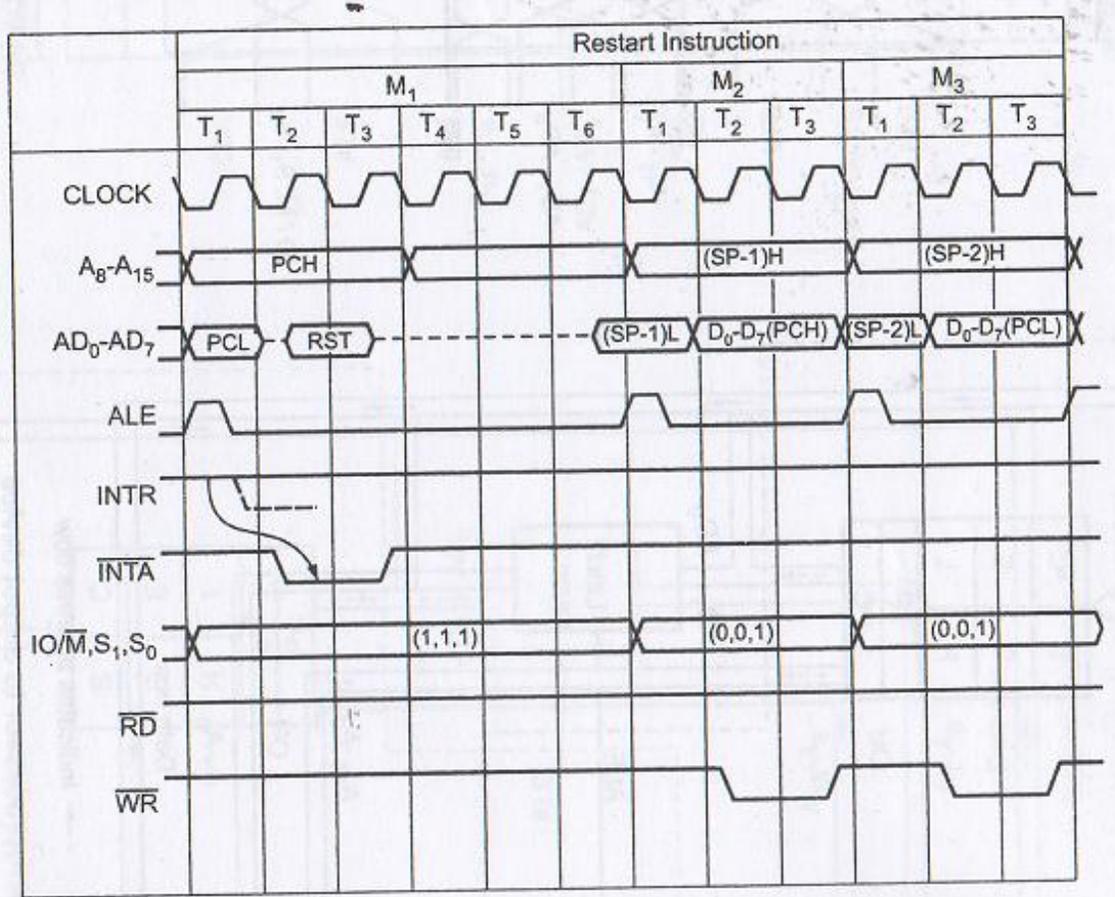


Figure 9.15: Timing diagram of the Restart instruction.

- ❖ Interrupt Acknowledge Cycle for CALL Instruction
The fetching and executing cycle of CALL instruction are shown in Fig. 9.16. Firstly, the two bytes of Called address will be fetched through two additional interrupt acknowledge machine cycles (M_2 and M_3 of Fig. 9.16). Secondly, The machine cycles M_4 and M_5 are memory write cycles that store the contents of the program counter on the stack memory, and then the new instruction cycle begins.

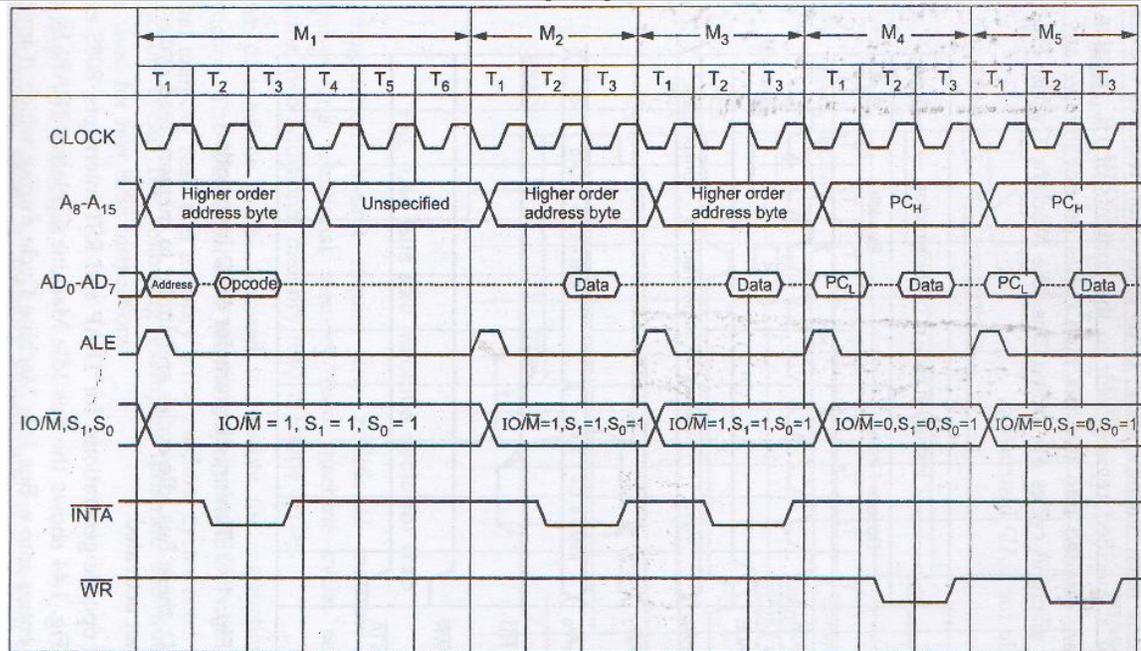


Figure 9.16: Timing diagram of INTA machine cycle and execution of CALL instruction.

9.3.7 Bus Idle Machine Cycle:

There are few situations where the machine cycles are neither Read and Write. These situations are:

DAD instruction which add the contents of register pair to HL registers and save the results in HL. This instruction required 10 T-states for opcode fetching machine cycle, and the other six T-states. Four for adding operation into two machine cycle without any reading or writing operations. The last two machine cycles of DAD instruction called Bus Idle machine cycles as shown in Fig. 9.17.

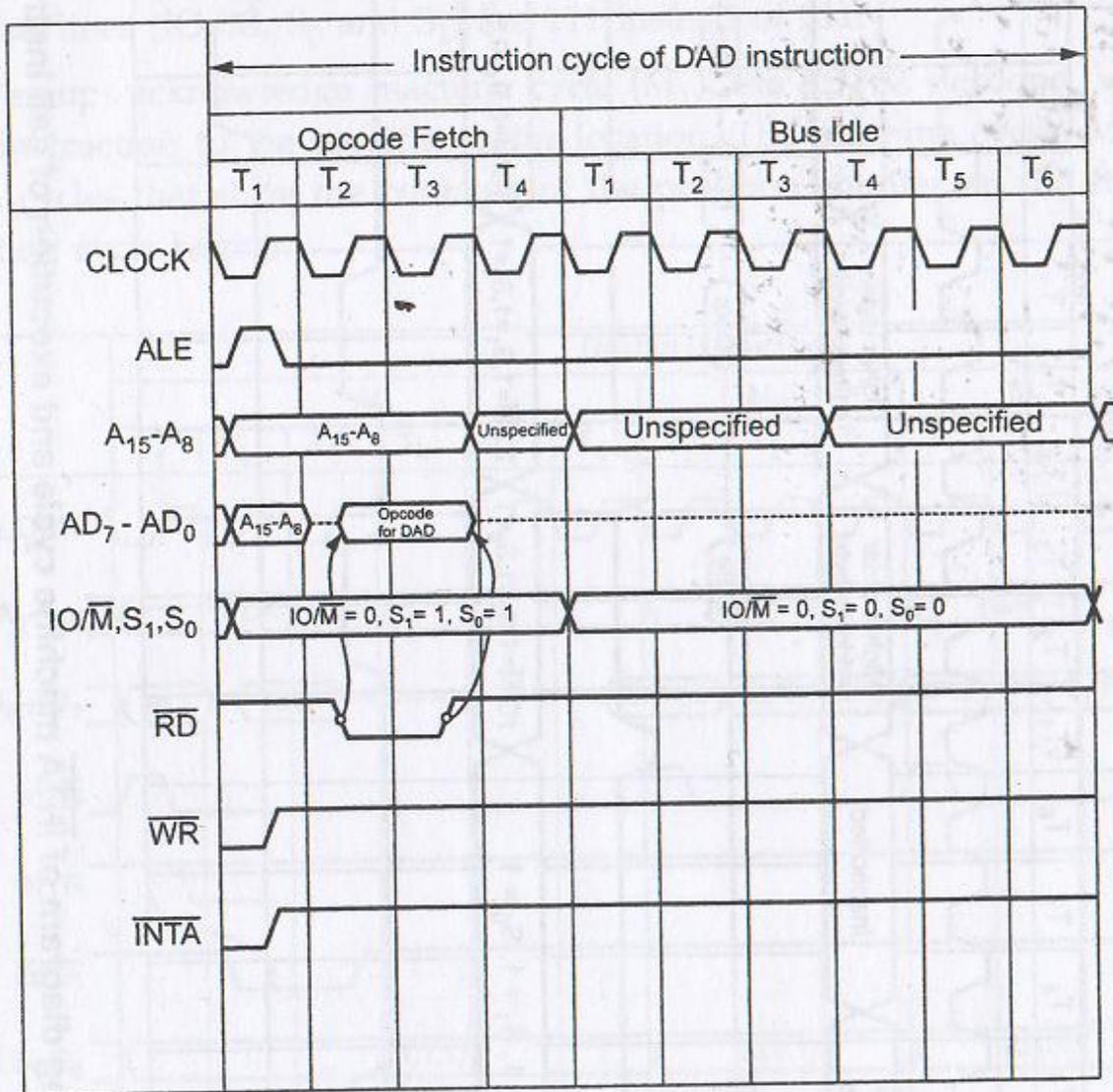


Figure 9.17: Timing diagram for DAD instruction.

Example1:

Draw and explain the timing diagram of **MOV B,C** instruction.

T₁ : The 1st clock of 1st machine cycle (M1) makes ALE high indicating address latch enabled which loads low-order address (00 H) on AD₇ \Leftrightarrow AD₀ and high-order address (10 H) simultaneously on A₁₅ \Leftrightarrow A₈. The address 00H is latched in T₁.

T₂ : During T₂ clock, the microprocessor issues \overline{RD} control signal to enable the memory and memory places 41H from 1000H location on the data bus.

T₃ : During T₃, the 41H is placed in the instruction register and $\overline{RD} = 1$ (high) disables signal. It means the memory is disabled in T₃ clock cycle. The opcode cycle is completed by end of T₃ clock cycle.

T4 : The opcode is decoded in T4 clock and the action as per 41H is taken accordingly. In other word, the content of C-register is copied in B-register as shown in Fig.9.18 below. Execution time for opcode 41H is:

Clock frequency of 8085 = 3.125 MHz

Time (T) for one clock = $1/3.125 \text{ MHz} = 0.32 \mu\text{S}$

Execution time for opcode fetch = $4T = 4 * 0.32 \mu\text{S} = 1.28 \mu\text{S}$.

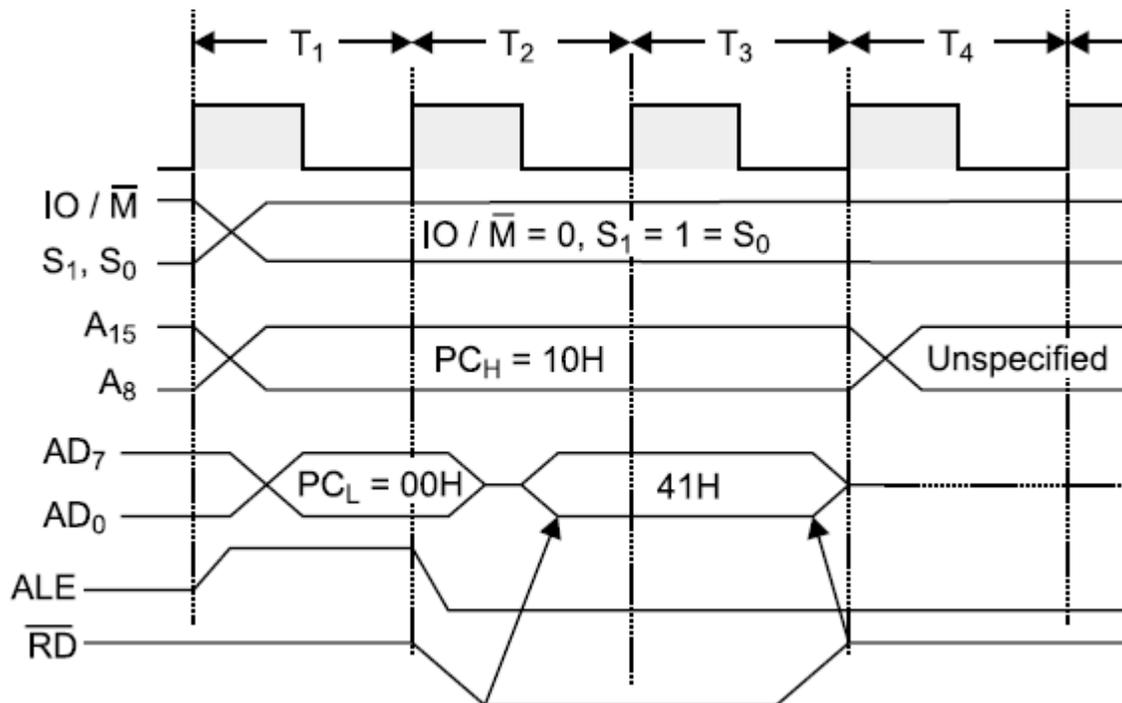


Figure 9.18: Timing diagram for MOV B,C instruction.

Example2:

The **MVI B,05H** instruction requires 2-machine cycles (M1 and M2). M1 requires 4-states and M2 requires 3-states, total of 7-states as shown in Fig. 9.19. Status signals $\overline{IO/M}$, S₁ and S₀ specifies the 1st machine cycle as the op-code fetch.

T1: The high order address {10H} is placed on the bus A₁₅ ⇔ A₈ and low-order address {00H} on the bus A_{D7} ⇔ A_{D0} and ALE = 1.

T2: The \overline{RD} line goes low, and the data 06H from memory location 1000H are placed on the data bus. The fetch cycle becomes complete in.

T3: The instruction is decoded.

T4: During T4-state, the contents of the bus are unknown.

With the change in the status signal, $\overline{IO/M} = 0$, S₁ = 1 and S₀ = 0, the 2nd machine cycle is identified as the memory read. The address is 1001H and the data byte [05H] is fetched via the data bus. Both M1 and M2 perform memory read operation, but the M1 is called op-code fetch i.e., the 1st machine cycle of each instruction is identified as the opcode fetch cycle. Execution time for MVI B,05H i.e., instruction cycle time is:

<i>Mnemonic</i>	<i>Instruction Byte</i>	<i>Machine Cycle</i>	<i>T-states</i>
MVI B,05H	Opcode	Opcode Fetch	4
	Immediate Data	Read Immediate Data	3
			<hr style="width: 20%; margin: 0 auto;"/> 7

Clock frequency of 8085 = 3.125 MHz

Time (T) for one clock = $1/3.125 \text{ MHz} = 0.32 \mu\text{S}$.

Time for Opcode Fetch = $4T = 4 * 0.320 \mu\text{S} = 1.28 \mu\text{S}$.

Time for Memory Read = $3T = 3 * 0.320 \mu\text{S} = 0.96 \mu\text{S}$.

Total Execution time for Instruction = $1.28 + 0.96 = 2.24 \mu\text{S}$.

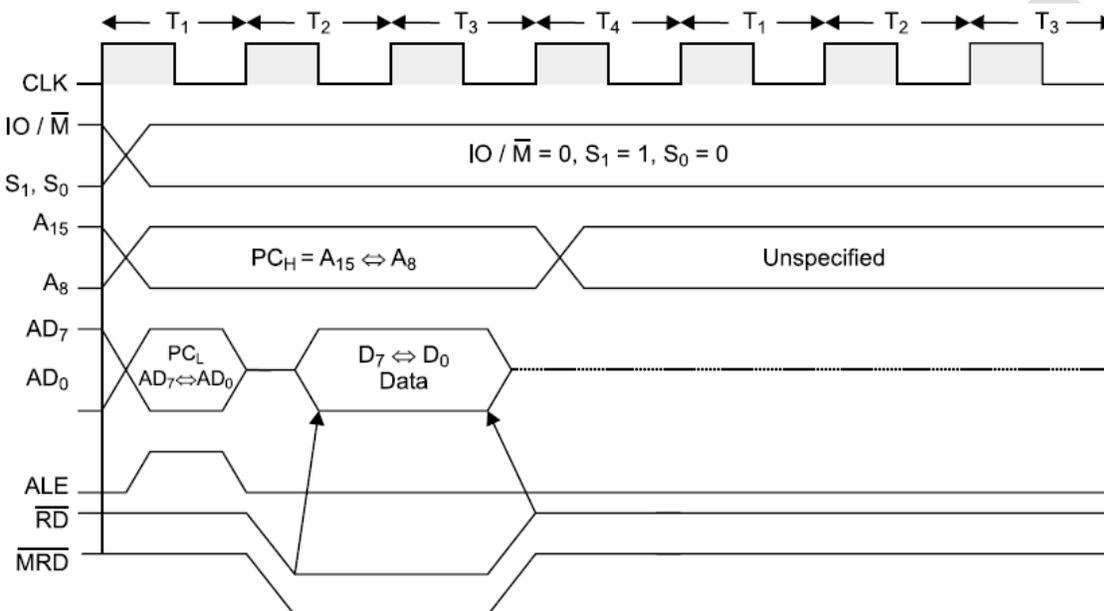


Figure 9.19: Timing diagram for MVI B,05 instruction.

Example3: Draw and explain the timing diagram of STA instruction

Solution: The STA instruction stands for storing the contents of the accumulator to a memory location whose address is immediately available after the instruction (STA). The 8085 have 16-address lines, it can address $2^{16} = 64 \text{ K}$. Since the STA instruction is meant to store the contents of the accumulator to the memory location, it is a 3-byte instruction. 1st byte is the opcode, the 2nd and 3rd bytes are the address of the memory locations. The storing of the STA instruction in the memory locations is as Opcode 1st byte Low address 2nd byte High address 3rd byte Three machine cycles are required to executing this instruction : opcode Fetch transfers the opcode from the memory to the instruction register. The 2-byte address is then transferred, 1-byte at a time, from the memory to the temporary register. This requires two Memory read machine cycles. When the entire instruction is in the microprocessor, it is executed. The execution process transfers data from the microprocessor to the memory. The contents of the accumulator are transferred

to memory, whose address was previously transferred to the microprocessor by the preceding 2-Memory Read machine cycles. The address of the memory location to be written is generated as

<i>Mnemonic</i>	<i>Instruction Byte</i>	<i>Machine Cycle</i>	<i>T-states</i>
STA	Opcode	Opcode Fetch	4
	LOW Address	Memory Read	3
	HIGH Address	Memory Read	3
		Memory Write	<u>3</u>
			13

The high order address byte in the temporary register is transferred to the address latch and the low order address byte is transferred to the address/data latch. This data transfer is affected by a Memory Write machine cycle. Thus 3-byte STA instruction has four machine cycles in its instruction cycle. The timing and control section of the microprocessor automatically generates the proper machine cycles required for an instruction cycle from the information provided by the opcode. The timing diagram of the instruction STA is shown in Fig. 9.20. The status of $\overline{IO/\overline{M}}$, S_1 and S_0 for 4-machine cycles are obtained from Table 9.1. The condition of $\overline{IO/\overline{M}}$, S_1 and S_0 would be 0, 1 and 1 respectively in MC1. The status of ALE is high at the beginning of 1st state of each machine cycle so that $AD7 \Leftrightarrow AD0$ work as the address bus. \overline{RD} remains high during 1st state of each machine cycle, since during 1st state of each machine cycle $AD7 \Leftrightarrow AD0$ work as address bus. It remains high during 4th state of the 1st machine cycle also as the 4th state is used to decode the op code for generating the required control signals. The opcode fetch of STA instruction has 4-states (clock cycles). Three states have been used to read the opcode from the main memory and the 4th to decode it and set up the subsequent machine cycle. The action of memory read or write cycles containing 3-states i.e., T_1 , T_2 , and T_3 are explained as

T_1 : During this period the address and control signals for the memory access are set up.

T_2 : The μP checks up the READY and HOLD control lines. If READY = 0, indicating a slow memory device, the μP enters in the wait state until READY = 1, indicating DMA request, then only the μP floats the data transfer lines and enters into wait until HOLD = 0.

T_3 : In memory read cycles the μP transfers a byte from the data bus to an internal register and in memory write cycle the μP transfers a byte from an internal register to the

data bus. Thus STA instruction requires 4-machine cycles containing 13-states (clock cycles). With a typical clock of 3 MHz (= 330 ns), the STA instruction requires 13*330 ns = 4.29 ms for its execution.

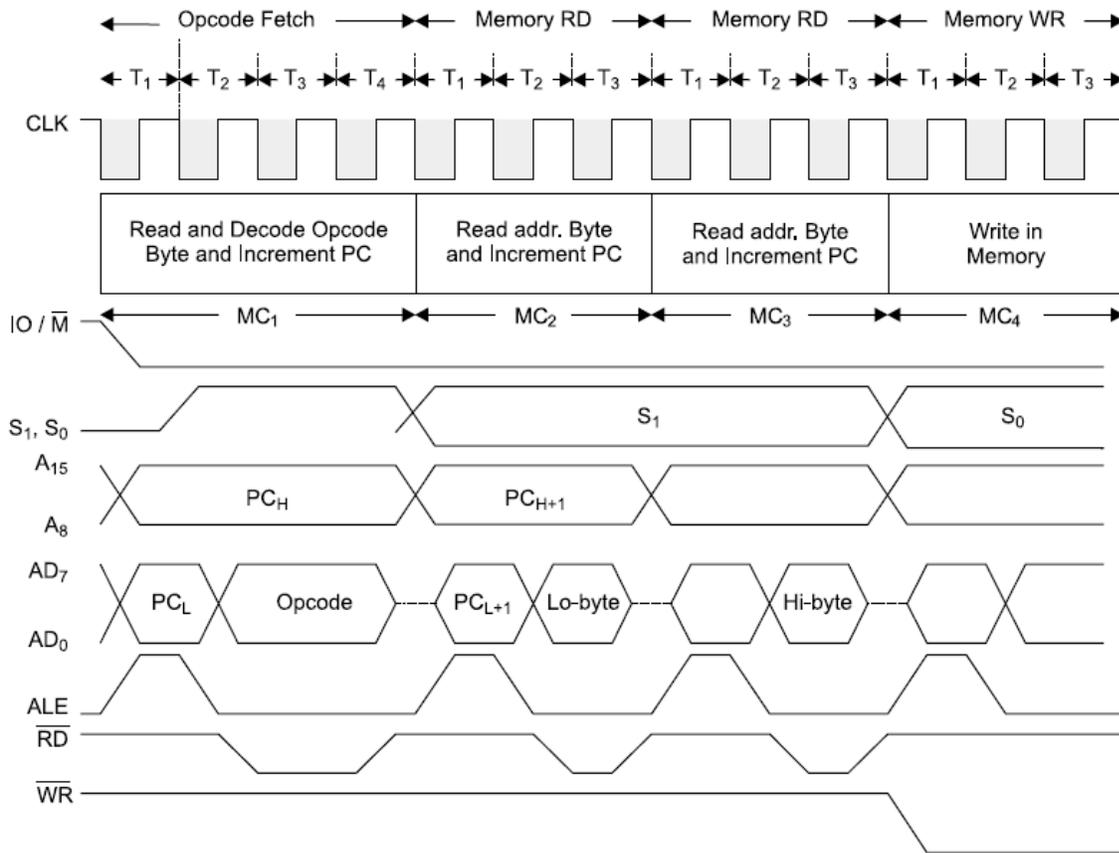


Figure 9.20: Timing diagram for STA instruction.