OP-AMP and its applications

Introduction

- The operational amplifier (Op-Amp) concept was introduced by Tellegen in 1954 under the name of "ideal amplifier". The first Op-Amps with discrete transistors appeared in production in 1956. One of the first analog ICs was an Op-Amp developed by R. Widlar in 1964. The operational amplifier is still the integrated circuit with highest production volume.
- OP-AMP is a very high-gain directly-coupled negative-feedback amplifier which can amplify signals having frequency ranging from **0 Hz to 1 MHz.**
- OP-AMP is so named because it was originally designed to perform mathematical operations like summation, subtraction, multiplication, differentiation integration …etc. Present day usage is much wider in scope but the popular name OP-AMP continues.

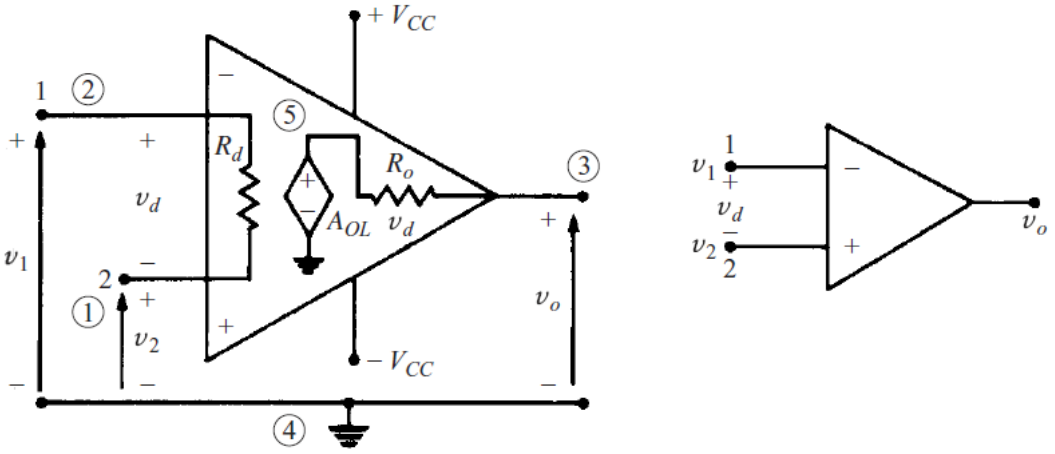
nd in analog computers applications.

- Typical applications of OP-AMP are scale changing, analog computer operations, in instrumentation and control systems and a great variety of phase-shift and oscillator circuits.
- Example of OP-AMPs [LM 108, LM 208, 741,….]

OP-AMP Circuit and Symbol

Standard triangular symbol of an OP-AMP is shown in Fig.1. All OP-AMPs have a minimum of five terminals:

1. inverting input terminal (labeled with a minus sign),
2. non-inverting input terminal (labeled with a plus sign),
3. output terminal,
4. positive bias supply terminal,
5. negative bias supply terminal.



(*a*) Complete representation (*b*) Simplified representation

Fig. 1: Operational amplifier

- When an OP-AMP is operated without connecting any resistor or capacitor from its output to any one of its inputs (*i.e.*, without feedback), it is said to be in the **open-loop condition**. The specifications of OP-AMP under such condition are called open-loop specifications and exhibiting the open-loop voltage gain (A_{OL}).
- An op amp amplifies the difference between two input signals v_1&v_2; i.e amplifies (v_d), where ($v_d=v_1-v_2$)

$v_o = A_{OL} * v_d$ (A_{OL} for actual op amp is extremely high *i.e.*, about 10^6)

However, if (v_d=1 V), it does not mean that will be amplified to 10^6 V at the output.

Actually, the maximum value of v_o is limited by the basis supply voltage and is called its ***saturation voltage***. This voltage is approximately 2V smaller than the power-supply voltage (V_{CC}). In other words, the amplifier is linear over the range

$-(V_{CC} - 2) < v_o < V_{CC} - 2$, typically ± 15 V.

Example1: An op amp has saturation voltage Vsat =10 V, an open-loop voltage gain of -10^5, and input resistance of 100k. Find (a) the value of v_d that will just drive the amplifier to saturation and (b) the op amp input current at the starting of saturation.

Solution:

(a) $$v_d = \frac{\pm V_{osat}}{A_{OL}} = \frac{\pm 10}{-10^5} = \pm 0.1 \text{ mV}$$

(b) $$i_{in} = \frac{v_d}{R_d} = \frac{\pm 0.1 \times 10^{-3}}{100 \times 10^3} = \pm 1 \text{ nA}$$

Ideal Operational Amplifier

An ideal *OP-AMP* has the following characteristics :

1. its open-loop gain A_{OL} is ***infinite*** *i.e.*, $Av = -\infty$

2. its input resistance *Ri* (measured between inverting and non-inverting terminals) is ***infinite*** *i.e.*, $Ri = \infty\ \Omega$. This means that the input current $i = 0$.

3. its output resistance R_0 (seen looking back into output terminals) is ***zero*** *i.e.*, $R_0 = 0\ \Omega$. This means that v_0 is not dependent on the load resistance connected across the output.

4. it has ***infinite bandwith*** *i.e.*, it has flat frequency response from dc to infinity.

Virtual Ground and Summing Point

Fig. 2 shows an *OP-AMP* which *employs* ***negative feedback*** with the help of resistor R_f which feeds a portion of the output to the input. The concept of **virtual** ground arises from the fact that input voltage *vi* at the inverting terminal of the *OP-AMP* is forced to a small value (assumed zero). Hence, point *A* is essentially at ground voltage and is referred to as *virtual ground*. Obviously, ***it is not the actual ground.***

When v1 is applied, point *A* attains some positive potential and at the same time v_0 is brought into existence. Due to negative feedback, some fraction of the output voltage is fed back to point *A* antiphase with the voltage already existing there (due to v1). The algebraic sum of the two voltages is almost zero so that $vi \cong 0$. Obviously, *vi* will become exactly zero when **negative feedback voltage at A is exactly equal to the positive voltage produced by v1 at A.**

Another point worth considering is that there exists a virtual short between the two terminals of the *OP-AMP* because $vi = 0$. It is virtual because no current flows (remember $i = 0$) despite the existence of this short.

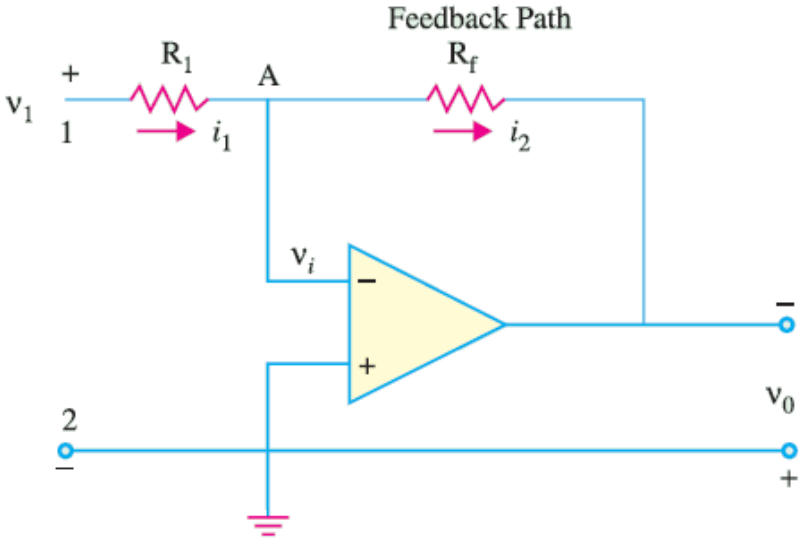


Fig. 2

OP-AMP Applications

1- Inverting Amplifier

The inverting amplifier of Fig. 3 has its noninverting input connected to ground. A signal (vin) is applied through input resistor R1, and negative current feedback is implemented through feedback resistor R_f . Output voltage (v_o) has polarity opposite that of input.

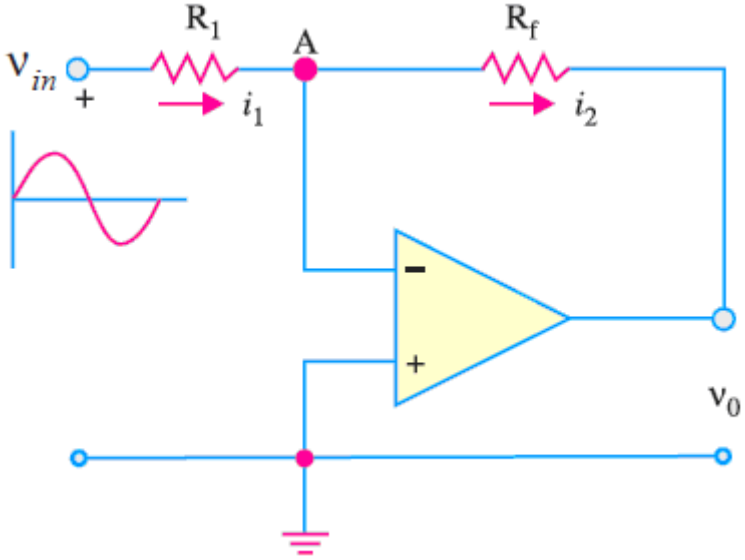


Fig. 3

The gain of the inverting amplifier can be driven as follow:
Since point *A* is at ground potential (V_A=0) and i_{in}=0,

$$i1=i2 \rightarrow \quad i_1=\frac{v_{in}-v_A}{R_1} \quad \text{and} \quad i_2=\frac{v_A-v_0}{R_f}$$

$$\frac{v_{in}-0}{R_1}=\frac{0-v_0}{R_f} \rightarrow \quad \frac{v_0}{R_f}=-\frac{v_{in}}{R_1} \quad \text{or} \quad \frac{v_0}{v_{in}}=-\frac{R_f}{R_1}$$

$$A_v=-\frac{R_f}{R_1} \qquad \text{Also, } v_0=-A_v v_{in}$$

It is seen from above, that closed-loop gain of the inverting amplifier depends on the ratio of the two external resistors *R*1 and *Rf* and is independent of the amplifier parameters.

2- Noninverting Amplifier

The noninverting amplifier of Fig. 4 is realized by grounding R1 of Fig. 3 and applying the input signal at the noninverting. Here, polarity of v0 is the same as that vin.

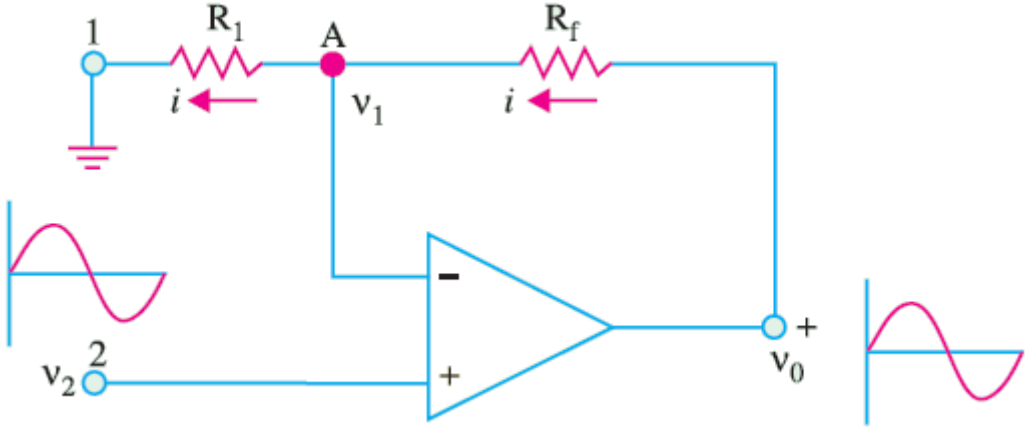


Fig. 4

The gain of the noninverting amplifier can be driven as follow:
Because of virtual short between the two *OP-AMP* terminals, voltage across *R*1 is the input voltage vin. Also, v0 is applied across the series combination of *R*1 and *Rf*.

$$\therefore \nu_{in} = iR_1 \quad , \nu_0 = i(R_1 + R_f)$$

$$A_\nu = \frac{\nu_0}{\nu_{in}} = \frac{i(R_1 + R_f)}{iR_1} \quad \text{or} \quad A_\nu = \frac{R_1 + R_f}{R_1} = \left(1 + \frac{R_f}{R_1}\right)$$

3- Voltage Follower

It provides a gain of unity without any phase reversal. This circuit (Fig. 5) is useful as a buffer or isolation amplifier because it allows, input voltage *vin* to be transferred as output voltage v0 while at the same time preventing load resistance *RL* from loading down the input source. It is due to the fact that its *Ri* = ∞ and *R*0 = 0.

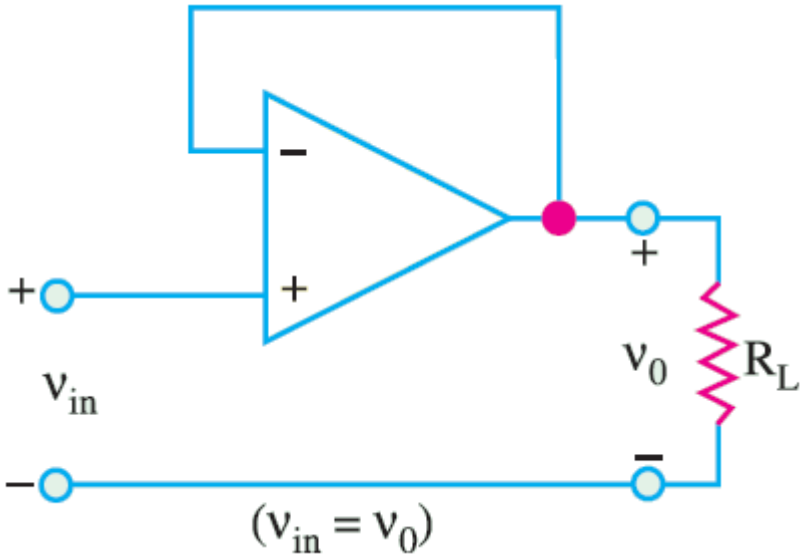


Fig. 5

4- Adder or Summer Amplifier

The adder circuit provides an output voltage proportional to or equal to the algebraic sum of two or more input voltages each multiplied by a constant gain factor. It is basically similar to a Fig. 3 except that it has more than one input. Fig. 6 shows a three-input inverting adder circuit. As seen, *the* ***output voltage is phase-inverted.***

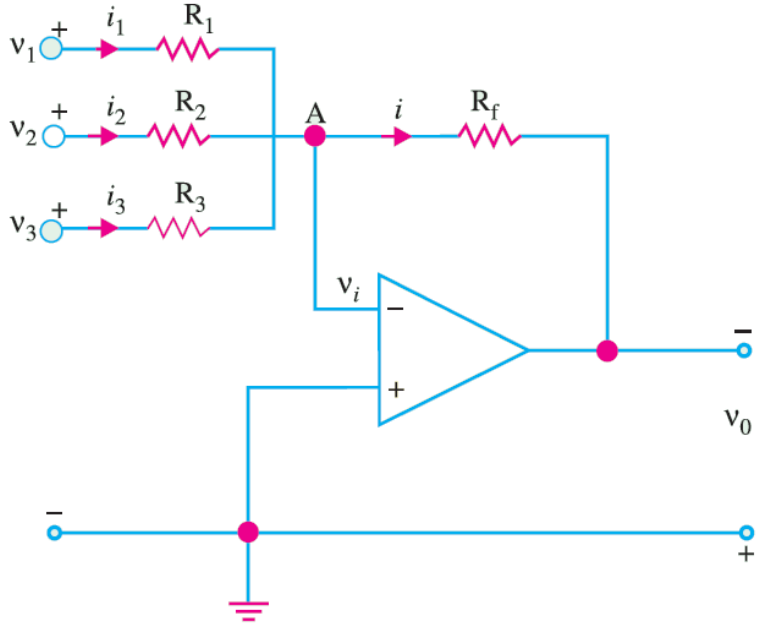


Fig. 6

Calculations

As before, we will treat point *A* as virtual ground

$$i_1 = \frac{v_1}{R_1}, \quad i_2 = \frac{v_2}{R_2}, \quad i_3 = \frac{v_3}{R_3} \quad \text{and} \quad i = -\frac{v_0}{R_f}$$

Applying *KCI* to point *A*, we have

$$i_1 + i_2 + i_3 + (-i) = 0$$

or $$\frac{v_1}{R_1} + \frac{v_2}{R_2} + \frac{v_3}{R_3} - \left(\frac{-v_0}{R_f}\right) = 0$$

$$\therefore \quad v_0 = -\left(\frac{R_f}{R_1} v_1 + \frac{R_f}{R_2} v_2 + \frac{R_f}{R_3} v_3\right)$$

If $R_1 = R_2 = R_3 = R$, then

$$v_0 = -\frac{R_f}{R}(v_1 + v_2 + v_3)$$

If $R_f = R$, then ouput exactly equals the sum of inputs.

5- Subtractor

The function of a subtractor is to provide an output proportional to the difference of two input signals. As shown in Fig. 7. The inputs are applying at the inverting and noninverting terminals.

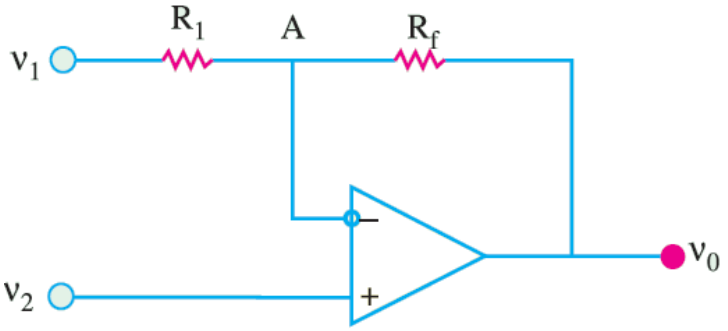


Fig. 7

Calculations

According to Superposition theorem;

$v0 = v0' + v0''$

where $v0'$ is the output produced by $v1$ and $v0''$ is that produced by $v2$.

Now $v_0' = -\frac{R_f}{R_1} \cdot v_1$ (see inverting amplifier equation)

$v_0'' = \left(1 + \frac{R_f}{R_1}\right) v_2$ (see noninverting amplifier equation)

If $Rf >> R1$ and $Rf/R1 >> 1$, hence

$$v_0 \cong \frac{R_f}{R_1}(v_2 - v_1)$$

Further, If $Rf = R1$, then

$v0 = (v2 - v1)$ = difference of the two input voltages

Example: Find the output voltages of an OP-AMP inverting adder for the following sets of input voltages and resistors. In all cases, Rf = 1 MΩ.

$v1 = -3$ V, $v2 = +3$V, $v3 = +2$V; R1 = 250 KΩ, R2 = 500 KΩ, R3 = 1 M Ω (ans. Vo=4v)

Example: In the subtractor circuit, R1 = 5 K, Rf = 10 K, $v1 = 4$ V and $v2 = 5$V. Find the value of output voltage.

Solution:

$$v_0 = \left(1 + \frac{R_f}{R_1}\right) v_1 - \frac{R_f}{R_1} v_2 = \left(1 + \frac{10}{5}\right) 4 - \frac{10}{5} \times 5 = +\mathbf{2V}$$

Example: Design an OP-AMP circuit that will produce an output equal to $-(4\,v1 + v2 + 0{\cdot}1v3)$. Write an expression for the output and sketch its output waveform when $v1 = 2 \sin \omega t$, $v2 = +5$V dc and $v3 = -100$ Vdc.

Solution:

$$v_0 = -\left[\frac{R_f}{R_1} v_1 + \frac{R_f}{R_2} v_2 + \frac{R_f}{R_3} v_3\right] \quad \ldots(1)$$

$$v_0 = -(4\,v_1 + v_2 + 0{\cdot}1\,v_3) \quad \ldots(2)$$

Comparing equations **(1)** and **(2)**, we find,

$$\frac{R_f}{R_1} = 4, \frac{R_f}{R_2} = 1, \frac{R_f}{R_3} = 0{\cdot}1$$

Therefore if we assume *Rf* = 100 *K*, then *R*1 = 25 *K*, *R*2 = 100 *K* and *R*3 = 10 *K*. With there values of *R*1, *R*2 and *R*3, the *OP-AMP* circuit is as shown in Fig. 8 (*a*).

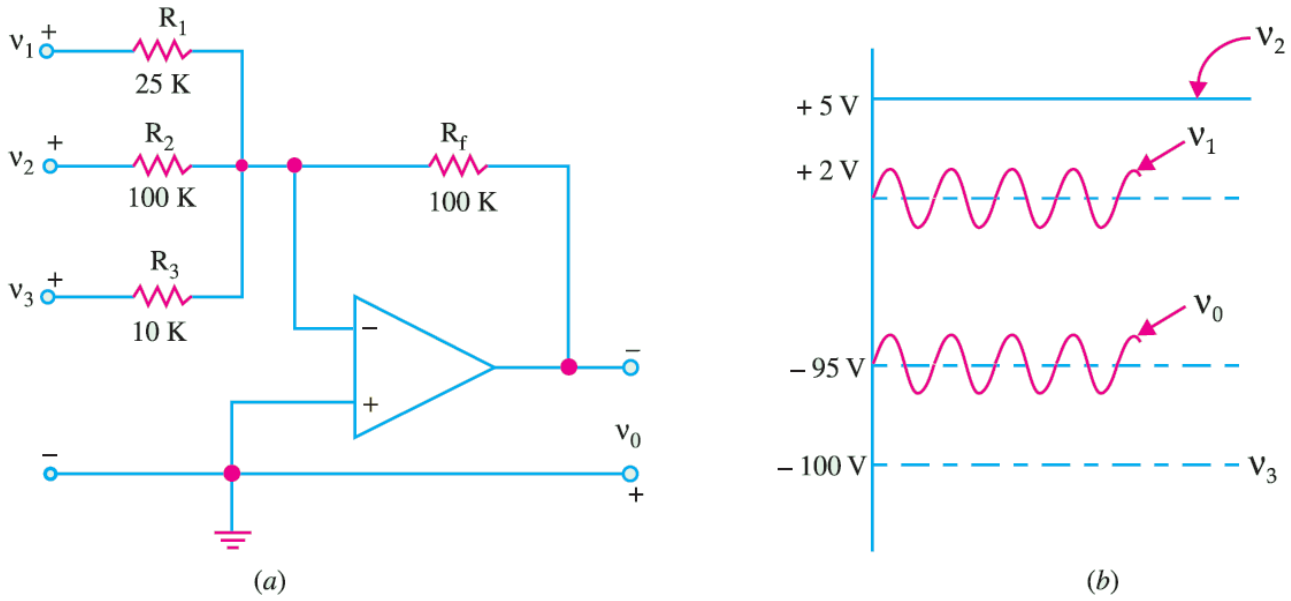


Fig. 8

With the given values of v1 = 2 sin ω*t*, v2 = + 5V, v3 = − 100 V dc, the output voltage, v0 = 2sin ω*t*+ 5 − 100 = 2 sin ω*t* − 95 V. The waveform of the output voltage is sketched as shown in Fig.8 (*b*).

6- Integrator

The function of an integrator is to provide an output voltage which is proportional to the integral of the input voltage. A simple example of integration is shown in Fig. 9, where input is dc level and its integral is ***a linearly-increasing ramp output.*** The actual integration circuit is similar to the inverting circuit except that **the feedback component is a capacitor C instead of a resistor R*f***.

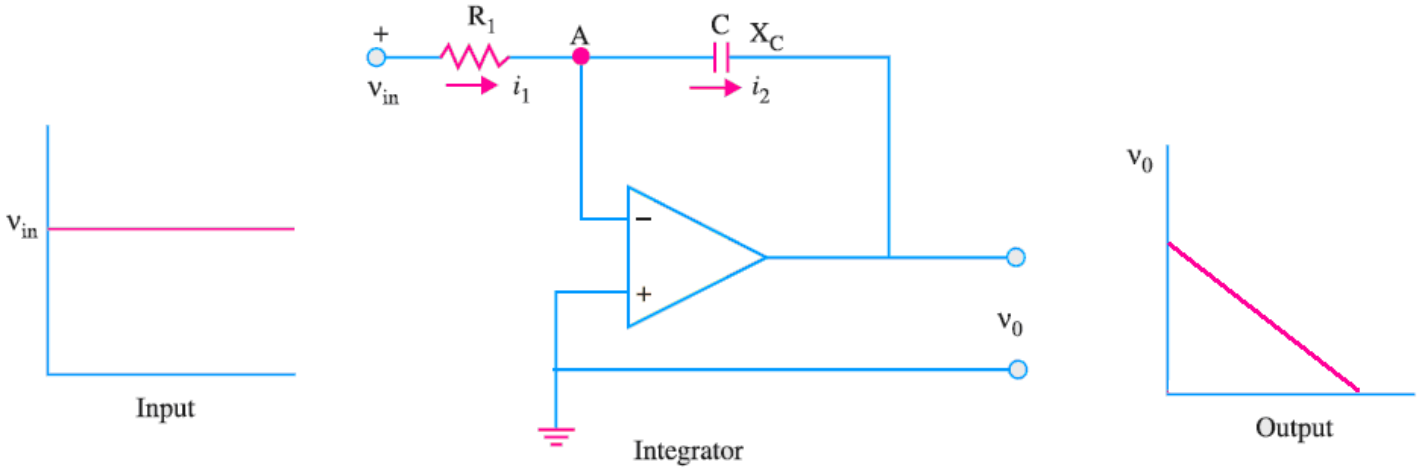


Fig. 9

Calculations

As before, If the op amp is ideal, point *A* will be treated as virtual ground, and v_{in} appears across R_1. Thus

$$i_1 = \frac{v_{in}}{R_1}$$

$$i_2 = i_c = c\frac{dv_c}{dt} = -c\frac{dv_o}{dt} \quad \text{(since } v_c = -v_o\text{)}$$

But, with negligible current into the op amp, the current through R1 = current flow through C. Then

$$\frac{v_{in}}{R_1} = -c\frac{dv_o}{dt} \rightarrow dv_0 = -\frac{1}{R_1 c}v_{in}dt \rightarrow v_o = -\frac{1}{R_1 c}\int v_{in}dt$$

It is seen from above that output (left-hand side) is an integral of the input, with an inversion and a scale factor of $1/CR_1$. This ability to integrate a given signal enables an analog computer solve differential equations and to set up a wide variety of electrical circuit analogs of physical system operation.

Note: we can integrate more than one input as shown below in Fig. 10. With multiple inputs, the output is given by

$$v_0(t) = -\left[K_1\int v_1(t)\,dt + K_2\int v_2(t)\,dt + k_3\int v_3(t)\,dt\right]$$

where $K_1 = \frac{1}{CR_1}$, $K_2 = \frac{1}{CR_2}$ and $K_3 = \frac{1}{CR_3}$

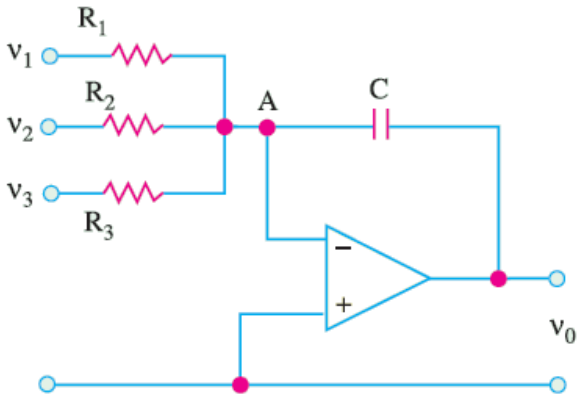


Fig. 10

Example: A 5mV, 1-kHz sinusoidal signal is applied to the input of an OP-AMP integrator, for which R = 100 K and C = 1 μF. Find the output voltage.

Solution:

$$-\frac{1}{CR} = \frac{1}{10^5 \times 10^{-6}} = -10$$

The equation for the sinusoidal voltage is

$$v_1 = 5\sin 2\pi ft = 5\sin 2000\,\pi t$$

Obviously, it has been assumed that at $t = 0$, $v_1 = 0$

$$v_0(t) = -10\int_0^t 5\sin 2000\,\pi t = -50\left|\frac{-\cos 2000\,\pi t}{2000}\right|_0^t$$

$$= -\frac{1}{40\,\pi}(\cos 2000\,\pi t - 1)$$

7- Differentiator

Its function is to provide an output voltage which is **proportional to the rate of the change of the input voltage.** It is an inverse mathematical operation to that of an integrator. As shown in

Fig. 11, when we feed a differentiator with linearly-increasing ramp input, we get a constant dc output.

Differentiator circuit can be obtained by interchanging the resistor and capacitor of the integrator circuit.

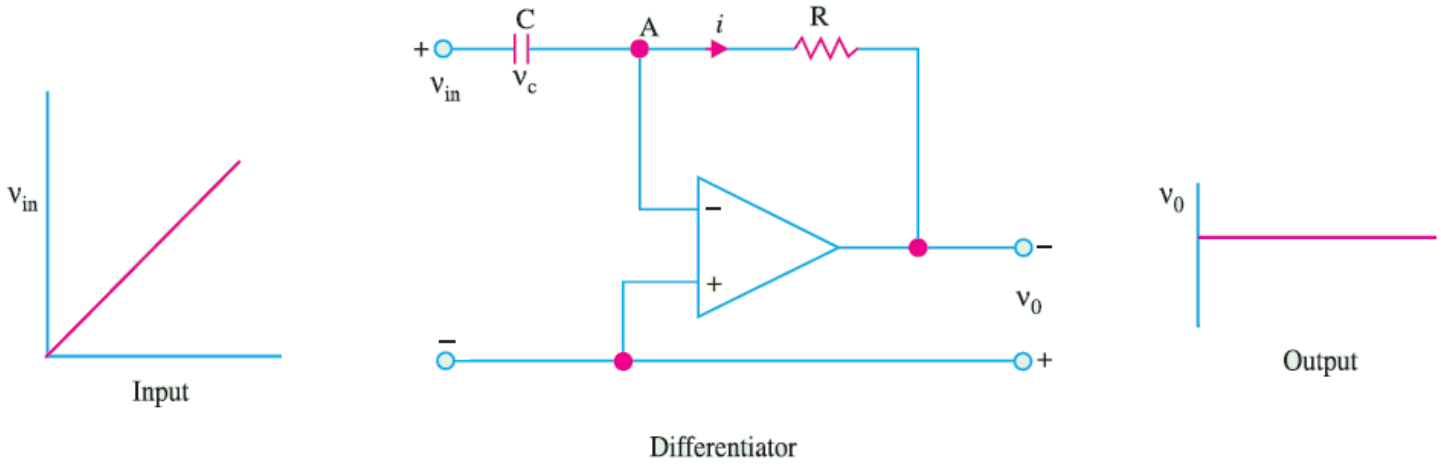


Fig. 11

Calculation:

The expression for the output signal of the inverting differentiator amplifier assuming the op amp is ideal can be derived as follows:

Taking point *A* as virtual ground, consequently, v_{in} appears across capacitor ($v_{in}=v_c$)

$$i = c\frac{dv_c}{dt} = -c\frac{dv_{in}}{dt}$$

$$v_o = -v_R = -iR = -c\frac{dv_{in}}{dt}R = -cR\frac{dv_{in}}{dt}$$

As seen, output voltage is proportional to the derivate of the input voltage, the constant of proportionality (*i.e.*, scale factor) being ($-RC$).

Example: The input to the differentiator circuit is a sinusoidal voltage of peak value of 5 mV and frequency 1 kHz. Find out the output if R = 1000 K and C = 1 μF.

Solution

The equation of the input voltage is $v1 = 5 \sin 2\pi \times 1000\, t = 5 \sin 2000\, \pi t$ mV

scale factor = $CR = 10^{-6} \times 10^5 = 0{\cdot}1$

$$v_0 = 0{\cdot}1\frac{d}{dt}(5 \sin 2000\, \pi t) = (0{\cdot}5 \times 2000\, \pi) \cos$$

dt (5 sin 2000 πt) = (0·5 × 2000 π) cos 2000 πt = 1000 π cos 2000 πt mV

As seen, output is a cosinusoidal voltage of frequency 1 kHz and peak value 1000 π mV.

8- Comparator

It is a circuit which compares two signals or voltage levels. The circuit is the simple because it needs no additional external components shown in Fig. 12. If v1 and v2 are equal, then v0 should ideally be zero.

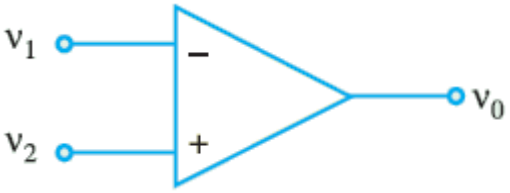


Fig. 12

Output of the comparator can be summarized as follows

If $V_1 > V_2$ then $V_o = -V_{cc}$ (Vsat)

If $V_1 < V_2$ then $V_o = V_{cc}$ (Vsat)

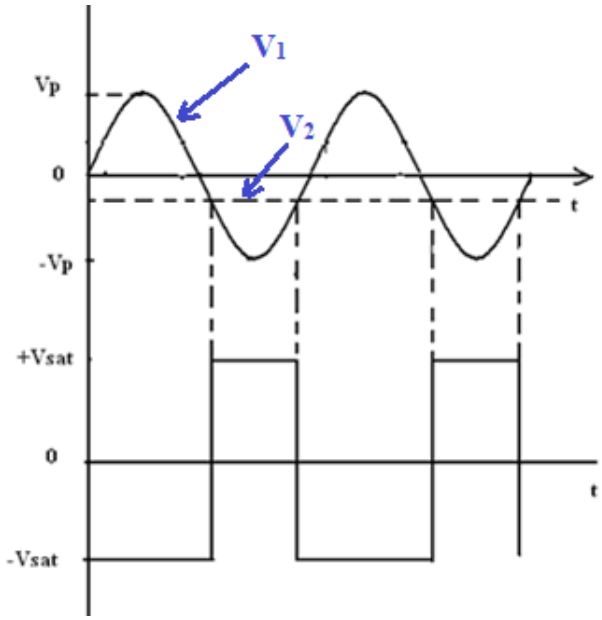


Fig. 13

Application of comparator

1- Zero Crossing Detector

Comparator can be used as a zero crossing detector. A typical circuit for such a detector is shown below:

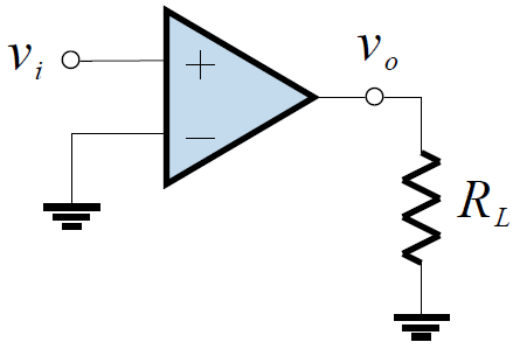


Fig. 14

During the positive half-cycle, the input voltage is positive, hence the output voltage is +*V*sat . During the negative half-cycle, the input voltage is negative, hence the output voltage is -*Vsat* . Thus the output voltage switches between +Vsat and -Vsat whenever the input signal crosses the zero level.

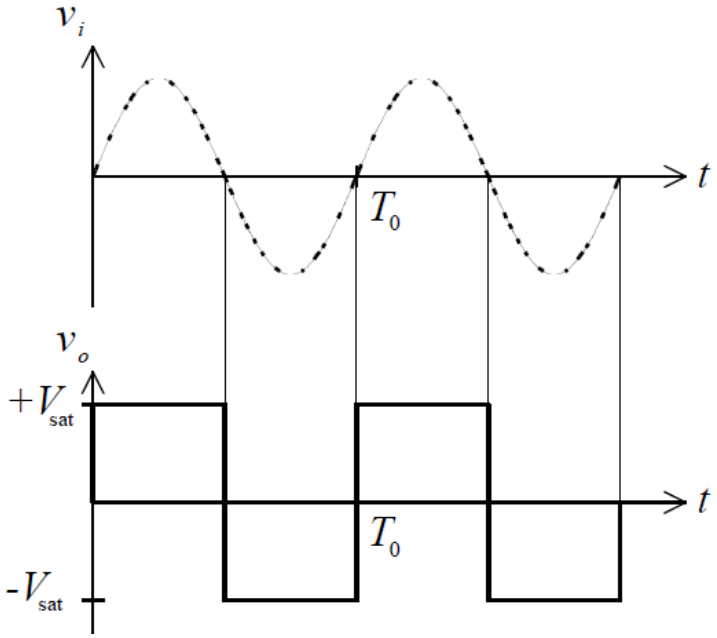


Fig. 15

Looking at the waveform shown above, we realize that a zero crossing detector can be used as a sine- to square-wave converter. This is an impractical circuit, since any noise on the input waveform near the zero crossings will cause multiple level transitions in the output signal (cause a comparator to erratically switch output states). In order to make the comparator less sensitive to noise, a comparator with positive feedback, called **hysteresis**, can be used. This comparator is called Schmitt trigger.

2- Output Bounding (or Voltage limiter)

In some applications, it is necessary to limit the output voltage levels of a comparator to a value less than the saturation voltage. A single zener diode can be used, as shown in Fig. 16, to limit the output voltage to the zener voltage in one direction and to the forward diode voltage drop in the other. This process of limiting the output range is called **bounding**.

The operation is as follows. Since the anode of the zener is connected to the inverting input, it is at virtual ground Therefore, when the output voltage reaches a positive value equal to the zener voltage, it limits at that value, as illustrated in Figure 17(a). When the output switches negative, the zener acts as a regular diode and becomes forward-biased at 0.7 V, limiting the negative output voltage to this value, as shown in part (b). Turning the zener around limits the output voltage in the opposite direction.

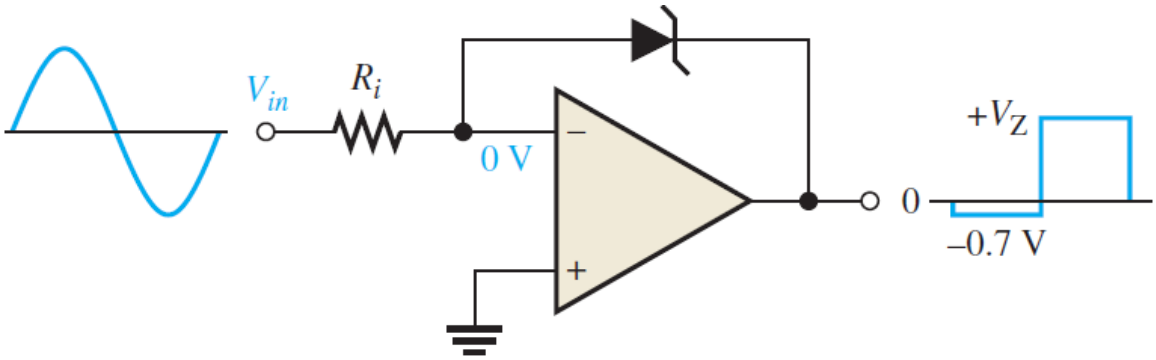


Fig. 17-(a) Bounded at a positive value

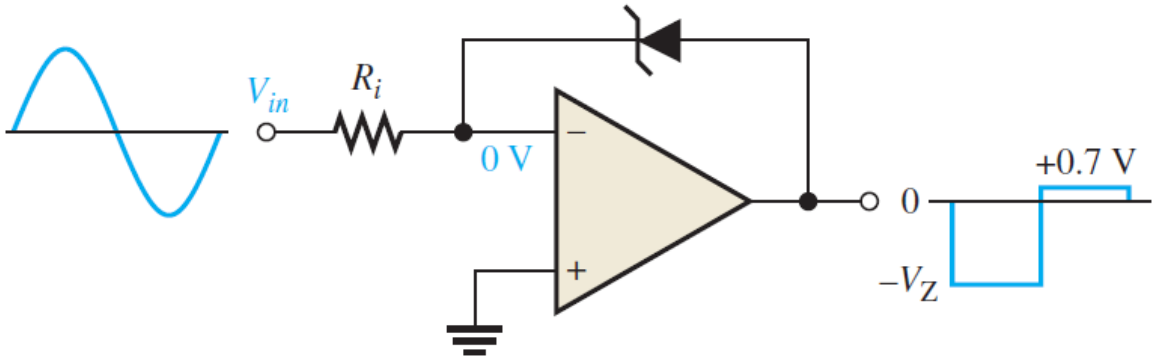


Fig. 17-(b) Bounded at a negative value

Two zener diode connected back to back with a comparator as in Fig. 18 to limit the output voltage to the zener voltage plus the voltage drop (0.7V) of the forward bias zener diode, both positively and negatively.

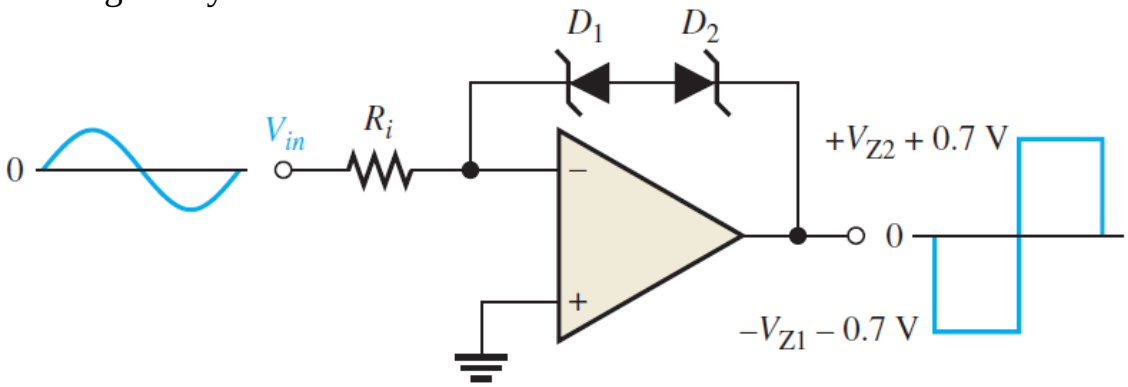


Fig. 18

9- Logarithmic and Antilog Amplifier

Log and antilog amplifiers are used in applications that require compression of analog input data, linearization of transducers that have exponential outputs, and analog multiplication and division. They are often used in high-frequency communication systems, including fiber optics, for processing wide dynamic range signals.

Note: The **logarithm** of a number is the power to which the base must be raised to get that number. A logarithmic (log) amplifier produces an output that is proportional to the logarithm of the input, and an antilogarithmic (antilog) amplifier takes the antilog or inverse log of the input.

a- Logarithmic Amplifier

The logarithmic amplifier is the use of a feedback-loop device that has an exponential terminal characteristic curve (diode or BJT transistor) which is characterized by

$$I_D = I_R(e^{V_D/V_T} - 1) \approx I_R e^{V_D/V_T} \qquad \text{.....(1)}$$

Where I_R is reverse leakage current, I_D is the forward diode current, V_D is the forward diode voltage (approximately 0.7 V), V_T is the thermal voltage and is a constant equal to approximately 25 mV at 25C^o.

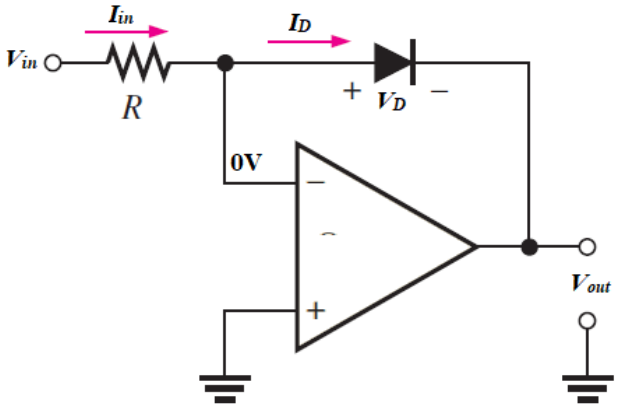


Fig. 19

An analysis of the circuit in Figure 19 is as follows, beginning with the facts that:

$$I_{in} = \frac{V_{in}}{R} = I_D \quad \text{.....(2)}$$

and $V_D = -V_o$ .....(3)

Substituting into the formula of eq. 1,

$$\frac{V_{in}}{R} = I_R e^{-V_{out}/V_T} \quad \rightarrow \quad V_{in} = RI_R e^{-V_{out}/V_T}$$

Take the natural logarithm (*ln*) of both sides

$$\ln(V_{in}) = \ln(RI_R e^{-V_{out}/V_T}) \Rightarrow \ln(V_{in}) = \ln(RI_R) - \frac{V_{out}}{V_T} \quad \text{.....(4)}$$

$$V_{out} = V_T[\ln(RI_R) - \ln(V_{in})] = -V_T \ln\frac{V_{in}}{RI_R} \quad \text{..... (5)}$$

Under the condition that the term RI_R is negligible (which can be accomplished by controlling R so that $RI_R \approx 1$, where the factor,I_R, is a constant for a given diode), then gives $V_{out} \approx -V_T \ln (V_{in})$.

Note: ***ln*** is the natural logarithm to the base *e*. A **natural logarithm** is the exponent to which the base ***e*** must be raised in order to equal a given quantity. Although eq. 5 will use natural logarithms in the formulas, each expression can be converted to a logarithm to the base 10(log10) using the relationship ln x = 2.3 log10x.

Example: Determine the output voltage for the log amplifier in Fig. 19. Assume I_R = 50nA and R=100k.

Solution:

$$V_{OUT} = -(0.025\text{ V})\ln\left(\frac{V_{in}}{I_R R}\right) = -(0.025\text{ V})\ln\left(\frac{2\text{ V}}{(50\text{ nA})(100\text{ k}\Omega)}\right)$$

$$= -(0.025\text{ V})\ln(400) = -(0.025\text{ V})(5.99) = \mathbf{-0.150\text{ V}}$$

Note1: The output voltage of the logarithmic amplifier is limited to a maximum value of approximately (-0.7V).

Note2: The input must be positive when the diode is connected in the direction shown in the Fig. 19. To handle negative inputs, the diode must be reversed.

Log Amplifier with a BJT

The base-emitter junction of a bipolar junction transistor exhibits the same type of logarithmic characteristic as a diode because it is also a *pn* junction. A log amplifier with a BJT connected in a common-base form in the feedback loop is shown in Figure 20. Notice that *Vout* with respect to ground is equal to $-V_{BE}$.

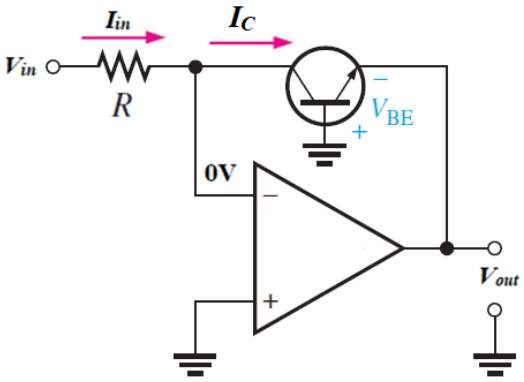


Fig. 20

The analysis for this circuit is the same as for the diode log amplifier except that V_{BE} replaces V_D, I_C replaces I_D and I_{BEO} replaces I_R. The expression for the V_{BE} versus I_C characteristic curve is

$$I_C = I_{EBO} e^{V_{BE}/V_T}$$

where I_{EBO} is the emitter-to-base leakage current. The expression for the output voltage is

$$V_{out} = -V_T \ln\left(\frac{V_{in}}{I_{EBO} R}\right)$$

b- Antilog Amplifier

The **antilogarithm** of a number is the result obtained when the base is raised to a power equal to the logarithm of that number. To get the antilogarithm, you must take the exponential of the logarithm (antilogarithm of $x=e^{lnx}$).

An antilog amplifier is formed by connecting a transistor (or diode) as the input element as shown in Fig. 21. The exponential formula still applies to the base-emitter *pn* junction. The output voltage is determined by the current (equal to the collector current) through the feedback resistor.

$$Vout = -R_f I_C$$

The characteristic equation of the *pn* junction is

$$I_C = I_{EBO} e^{V_{BE}/V_T}$$

Substituting into the equation for V_{out}

$$V_{out} = -R_f I_{EBO} e^{V_{BE}/V_T}$$

As you can see in Fig. 21, $V_{in} = V_{BE}$

$$V_{out} = -R_f I_{EBO} e^{V_{in}/V_T}$$

The exponential term can be expressed as an antilogarithm as follows:

$$V_{out} = -R_f I_{EBO} antilog\left(\frac{V_{in}}{V_T}\right)$$

Where V_T is approximately 25 mV.

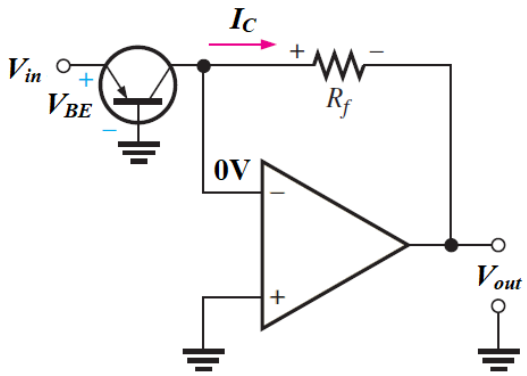


Fig. 21

Example: For the antilog amplifier in Figure 21, find the output voltage. Assume I_{EBO} = 40 nA, V_{in}=175.1 mV and Rf= 68k.

solution

$$V_{out} = -R_f I_{EBO}\text{antilog}\left(\frac{V_{in}}{25\text{ mV}}\right) = -(68\text{ k}\Omega)(40\text{ nA})\text{antilog}\left(\frac{175.1\text{ mV}}{25\text{ mV}}\right)$$

$$= -(68\text{ k}\Omega)(40\text{ nA})(1101) = \mathbf{-3\text{ V}}$$

Note: In certain applications, a signal may be too large in magnitude for a particular system to handle. In these cases, the signal voltage must be scaled down by a process called **signal compression** so that it can be properly handled by the system. If a linear circuit is used to scale a signal down in amplitude, the lower voltages are reduced by the same percentage as the higher voltages. Linear signal compression often results in the lower voltages becoming obscured by noise and difficult to accurately distinguish, as illustrated in Fig. 22-a. To overcome this problem, a signal with a large dynamic range can be compressed using a logarithmic response, as shown in Figure 22-b. In logarithmic signal compression, the higher voltages are reduced by a greater percentage than the lower voltages, thus keeping the lower voltage signals from being lost in noise.

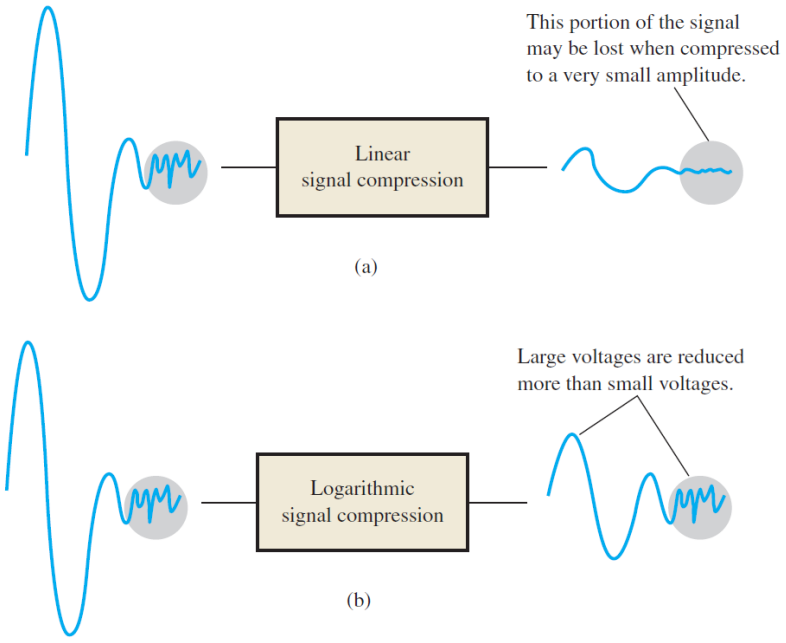


Fig. 22

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Questions

1. What purpose does the diode or transistor perform in the feedback loop of a log amplifier?
2. Why is the output of a log amplifier limited to about 0.7 V?
3. What are the factors that determine the output voltage of a basic log amplifier?
4. In terms of implementation, how does a basic antilog amplifier differ from a basic log amplifier?
5. Define the term *bounding* in relation to a comparator's output.
6. What is the reference voltage for each comparator in Figure 23?

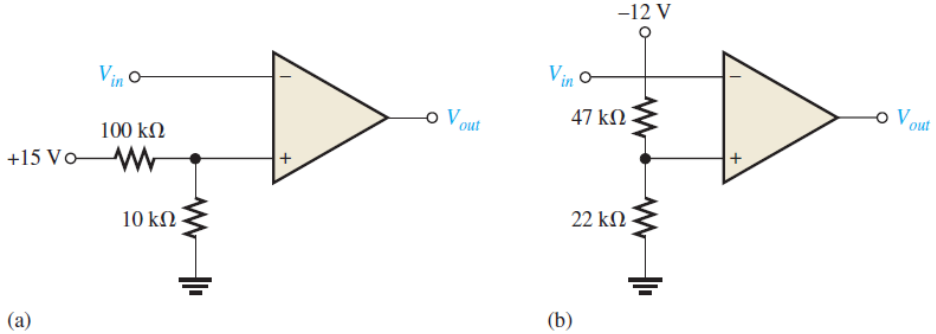


Fig. 23

Other OP-AMP Circuts

This section introduces other op-amp circuits that represent basic applications of the op-amp. These circuit, of course, not a comprehensive coverage of all possible op-amp circuits but is intended only to introduce some common basic uses.

1- Constant Current Source

A constant-current source delivers a constant current to the load even the load resistance changes. Figure 24 shows a basic circuit in which a voltage source (V_{IN}) provides a constant current (I_i) through the input resistor (R_i).

Since the inverting input of the op-amp is at virtual ground (0V), the value of (I_i) is determined by

$$I_i = \frac{V_{IN}}{R_i}$$

Now, since $Ii = I_L$

$$I_L = \frac{V_{IN}}{R_i}$$

If R_L changes, I_L remains constant as long as V_{IN} and R_i are held constant.

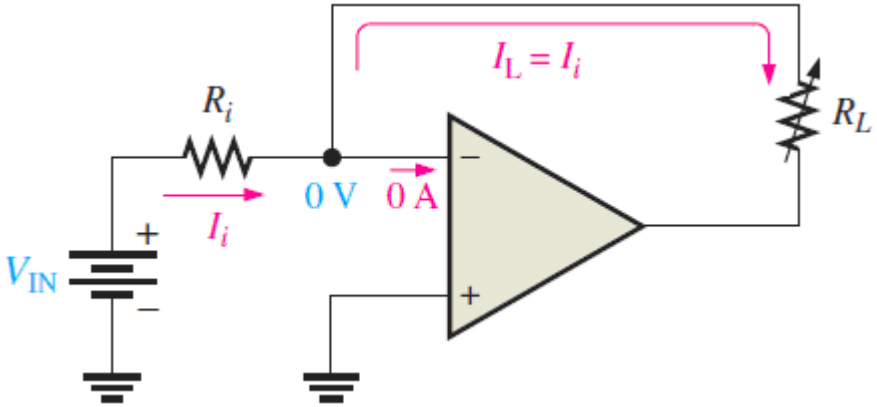


Fig. 24

2- Precision Rectifiers

Rectifier circuits can be implemented with silicon junction diodes. Recall that for the diode to conduct, the voltage across it must be ≈ 0.7 V. Therefore, a major limitation of these circuits is that they cannot rectify voltages below about 0.7 V. In addition, since the input voltage has to rise to about 0.7 V before any appreciable change can be seen at the output, the output is distorted as shown in Fig. 25.

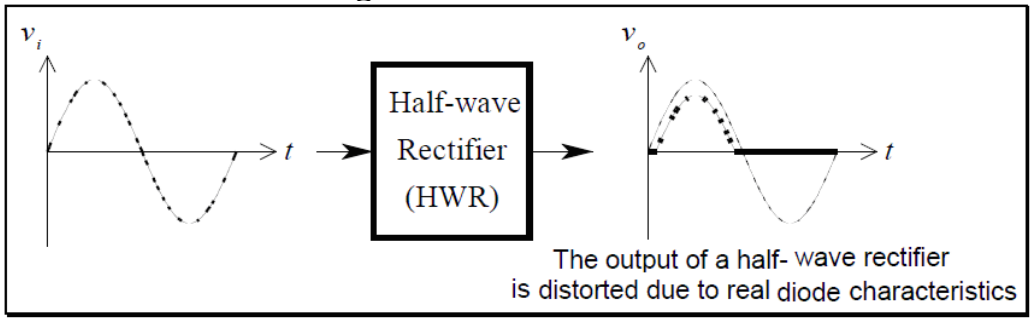


Fig. 25

- *half-wave rectifier* (HWR) is a circuit that passes only the positive (or only the negative) portion of a wave, while blocking out the other portion. The transfer characteristic of the positive HWR is:

$v_O = v_i$ for $v_i > 0$, $v_O = 0$ for $v_i < 0$.

- *full-wave rectifier* (FWR), besides passing the positive portion, inverts and then passes also the negative portion. Its transfer characteristic is:

$v_O = v_i$ for $v_i > 0$, $v_O = v_i$ for $v_i < 0$. or, more concisely, $v_O = |v_i|$

i- Half-Wave Rectifiers

Figure 26 below shows a precision half-wave rectifier circuit consisting of a diode placed in the negative-feedback path of an ideal op-amp.

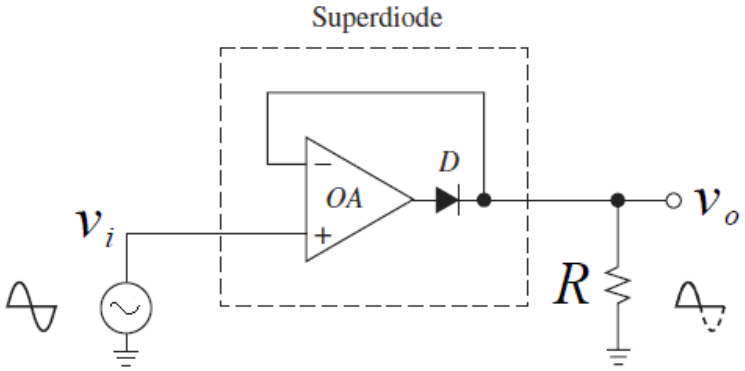


Fig. 26

The analysis of the circuit of Fig. 26 above is illustrated as below:

1- when input voltage is positive ($v_i > 0$), the op-amp output (v) will also positive, turning ON the diode and thus creating the negative-feedback path shown in Fig. 27-a. This allows op amp to operate as voltage follower and give $v_O = v_i$ (prove that). The output of the op amp (v) is a diode drop above v_O, ($v = v_O + V_{D(on)}$) $\approx v_O + 0.7$ V.

2- when input voltage is negative ($v_i < 0$): The op amp output (v) is negative, turning the diode OFF and thus causing the current through R to go to zero. Hence, v_O =0. As shown in Fig. 27-b, the op amp is now operating in the open-loop mode.

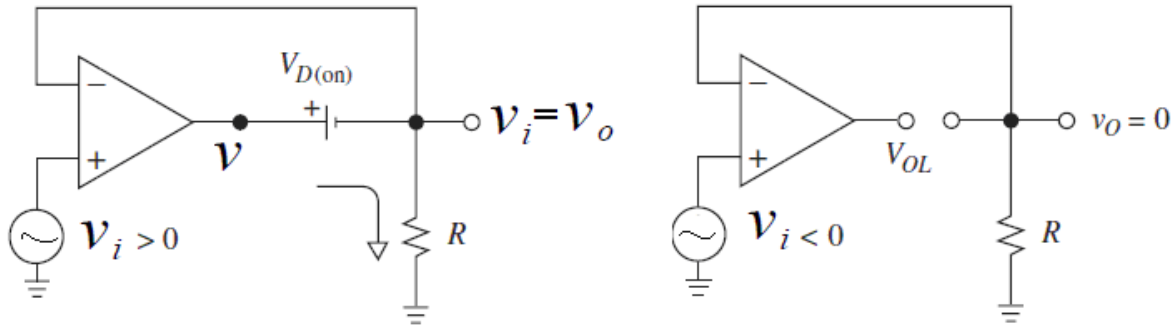


Fig. 27

A disadvantage of this circuit is that when v_i changes from positive to negative the op-amp will be saturated close to its negative supply rail. Thus, the op amp output may exhibit intolerable distortion. The improved HWR of Fig. 28 alleviates this inconvenience by using a second diode. Circuit operation is summarized as:

1- $v_i > 0$ ➔ $v_O = 0$. (positive input causes D_1 to conduct, thus creating a negative-feedback path around the op amp. By the virtual-ground, D_1 now clamps the op amp output at $v = -V_{D1(on)} \approx -0.7$ V. Moreover, D_2 is OFF, so no current flows through R_2 and, hence, $v_O = 0$).

2- $v_i < 0$ ➔ $v_O = v_i$. (negative input causes the op amp output positive, thus turning D_2 ON. This creates an alternative negative-feedback path via D_2 and R_2. Clearly, D_1 is now OFF, so the op amp operate as inverting amplifier, i.e. $v_O = (-R_2/R_1)v_i$).

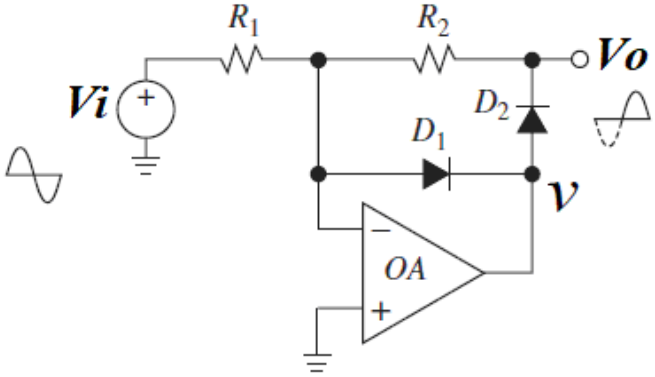


Fig. 28

Full-Wave Rectifiers

There are many configuration for achieving precision FWR. One of them is given in Fig. 29. Here op amp (OA1) provides inverting half-wave rectification, and op amp (OA2) sums v_i and the HWR output (v_{HW}) to give $v_O = -[(R_5/R_4)v_i + (R_5/R_3)v_{HW}]$.

Where $v_{HW} = -(R_2/R_1)v_i$ for $v_i > 0$, and $v_{HW} = 0$ for $v_i < 0$.

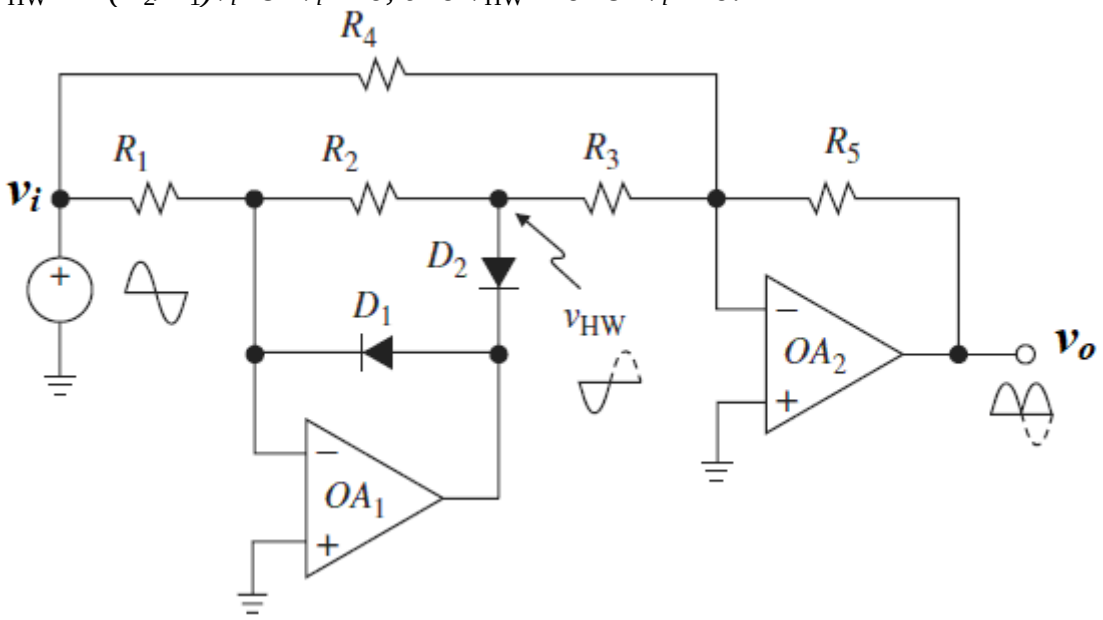


Fig. 29

Example1: Draw the output showing its proper relationship to the input signal of the comparator circuit shown in Fig.30. Assume the maximum output levels of the op-amp are ± 12V.

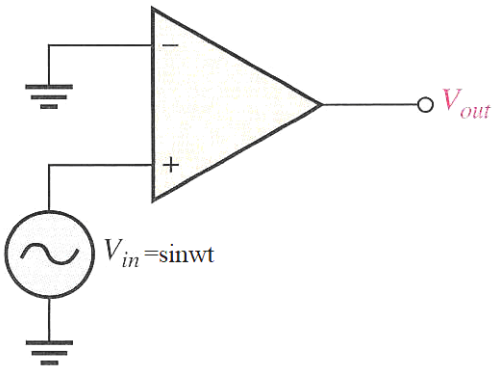


Fig.30

Solution:

When Vin > 0 ➔ Vout =+12 (maximum positive level)

When Vin > 0 ➔ Vout =-12 (maximum negative level)

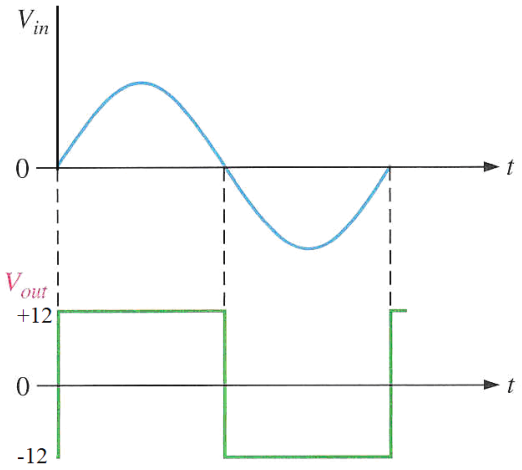


Fig. 40

Example2: Draw the output showing its proper relationship to the input signal of the comparator circuit shown in Fig.41. Assume the maximum output levels of the op-amp are ±12V.

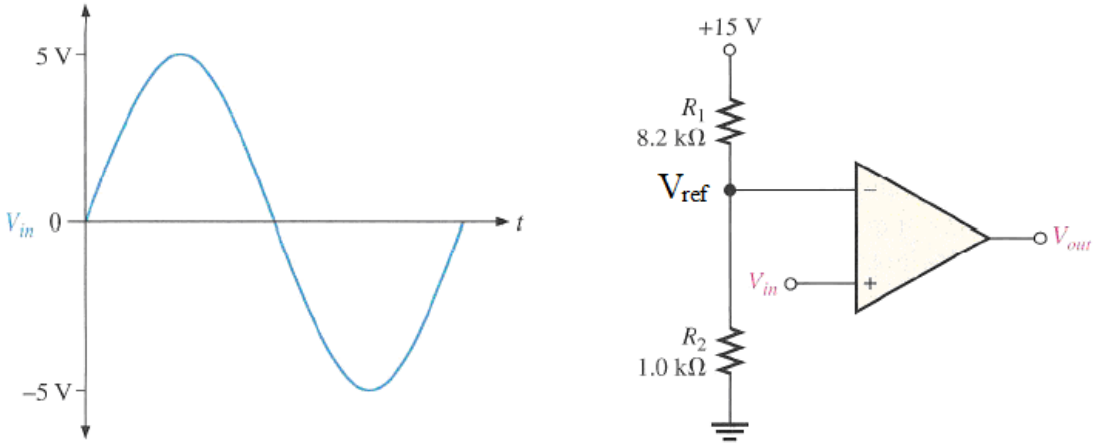


Fig.41

Solution:

The reference voltage (V_{REF}) is set by R_1 and R_2 (use voltage divider rule)

$$V_{REF} = \frac{R_2}{R_1 + R_2}(+V) = \frac{1.0\ \text{k}\Omega}{8.2\ \text{k}\Omega + 1.0\ \text{k}\Omega}(+15\ \text{V}) = 1.63\ \text{V}$$

As shown in Fig. 42, each time the input exceeds +1.63 V, the output voltage switches to its +12V level, and each time the input goes below +1.63 V, the output voltage switches to its -12V level.

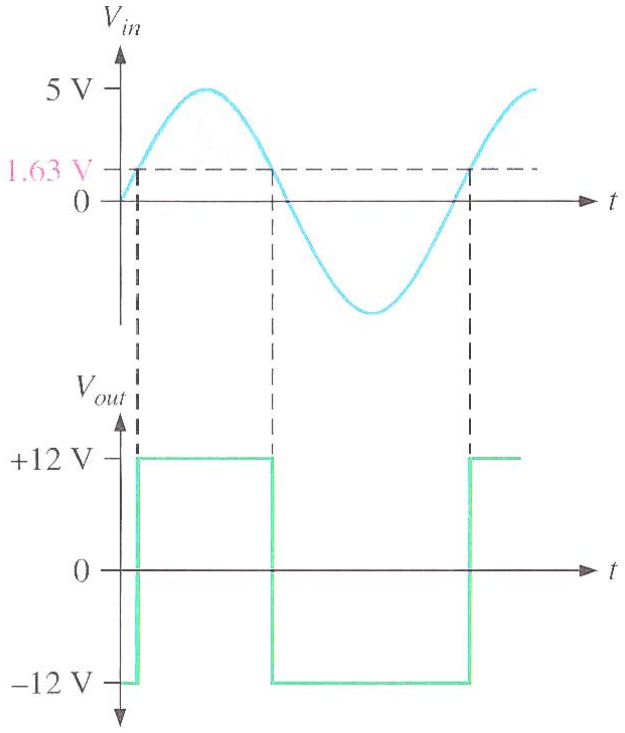


Fig. 42

Problem: Draw the output showing its proper relationship to the input signal of the comparator circuits shown in Fig.43. Assume the maximum output levels of the op-amp are ± 15V.

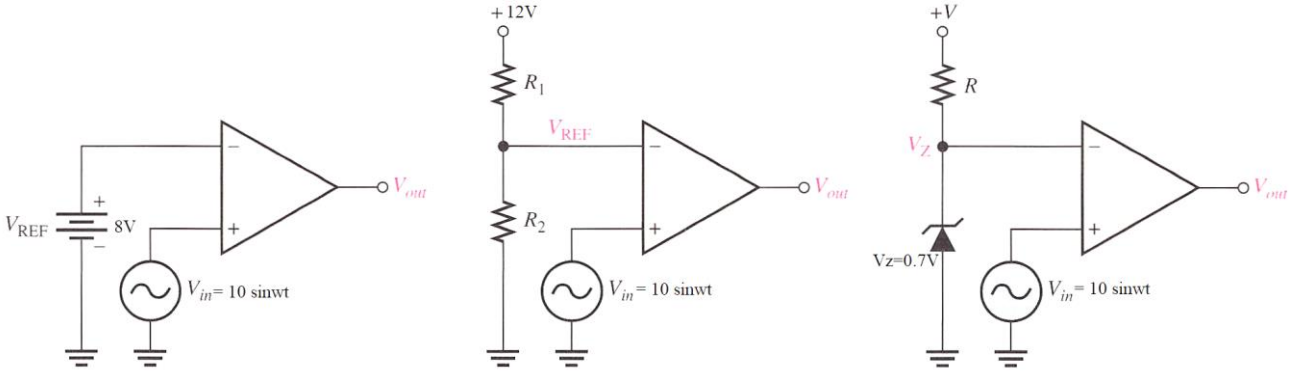


Fig. 43

Example3: Determine the output voltage response to the input square wave for the ideal integrator in Fig. 44. The output voltage is initially zero.

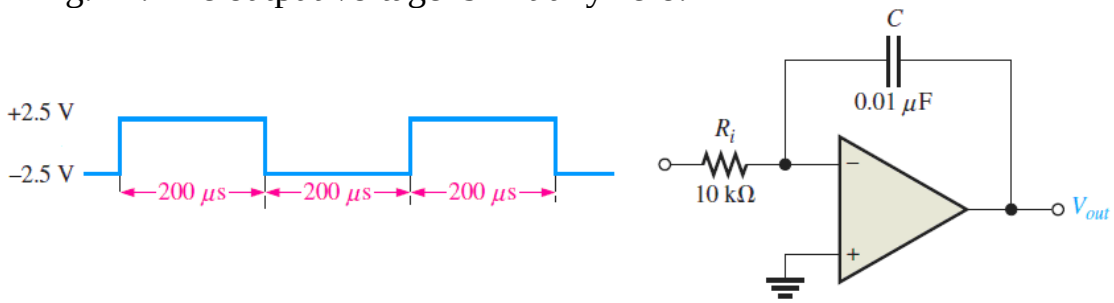


Fig. 44

Solution

The output voltage during the time that the input is at +2.5 V (capacitor charging) is

The output voltage during the time that the input is negative (capacitor discharging) is the same as during charging except it is positive.

When the input is at +2.5 V, the output is a negative-going ramp. When the input is at -2.5V the output is a positive-going ramp.
During the time the input is at +2.5 V, the output is a negative-going ramp (will go from 0 to -5). During the time the input is at -2.5V the output is a positive-going ramp (will go from -5 V to 0 V). Therefore, the output is a triangular wave with peaks at 0 and -5 as shown in Fig. 45.

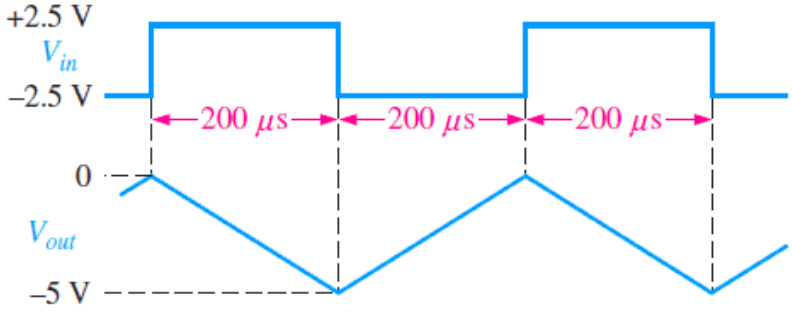


Fig. 45

Example: Determine the output voltage of the ideal op-amp differentiator in Fig.46 for the triangular-wave input shown.

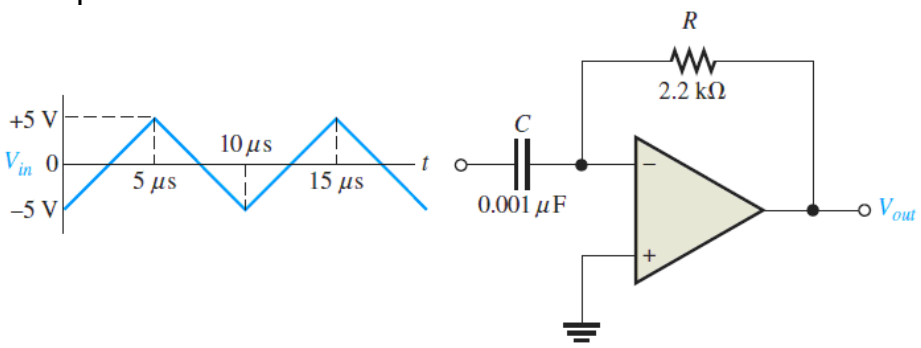


Fig.46

Solution

Starting at t= 0, the input voltage is a positive-going ramp ranging from -5V to +5V (+10V change) in 5μs. Then it changes to a negative-going ramp ranging is:

Time constant = RC = (2.2 kΩ) (0.001 μF) = 2.2 μs

And $$\frac{dV_{in}}{dt} = \frac{\Delta V_{in}}{\Delta t} = \frac{(-5-5)V}{(5-0)\mu s} = 2V/\mu s$$

$$V_{out} = -RC\frac{dV_{in}}{dt} = -2.2 \times 2 = -4.4V$$

Likewise, the slope of the negative-going ramp is -2V/μs and the output voltage is

$$V_{out} = -(-2.2 \times 2) = 4.4V$$

Figure 47 shows a graph of the output voltage waveform relative to the input.

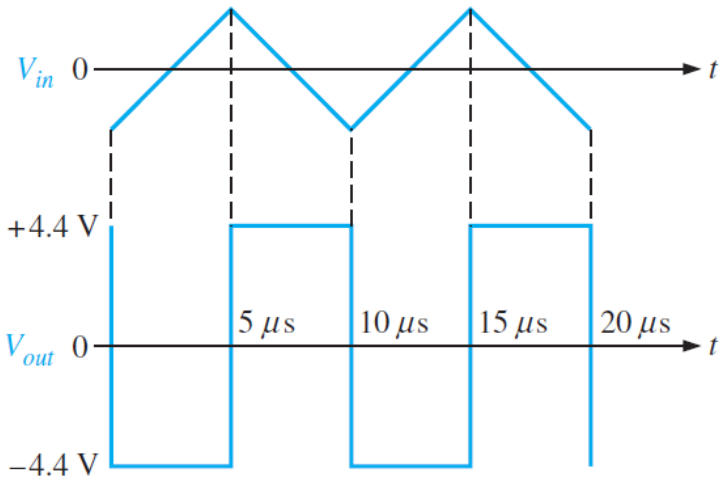


Fig. 47

ex:(1) Draw the output voltage of the integrator if the input voltage is square wave with 1KHZ frequancy and 10 p.p. ($R = 10K\Omega$, $C = 0.1\mu F$)

Solution :- $f = 1KHZ \Rightarrow t = \frac{1}{f} = \frac{1}{1000} = 1ms$

* for positive half cycle $V_{in} = +5$ Volt

$$V_o = -\frac{1}{RC}\int_0^{0.5ms} V_{in}\,dt = -\frac{1}{RC}\int_0^{0.5ms} 5\,dt = -\frac{5}{RC}t\Big|_0^{0.5} = \frac{-5*(0.5)}{10*10^3*0.1*10^{-6}}$$

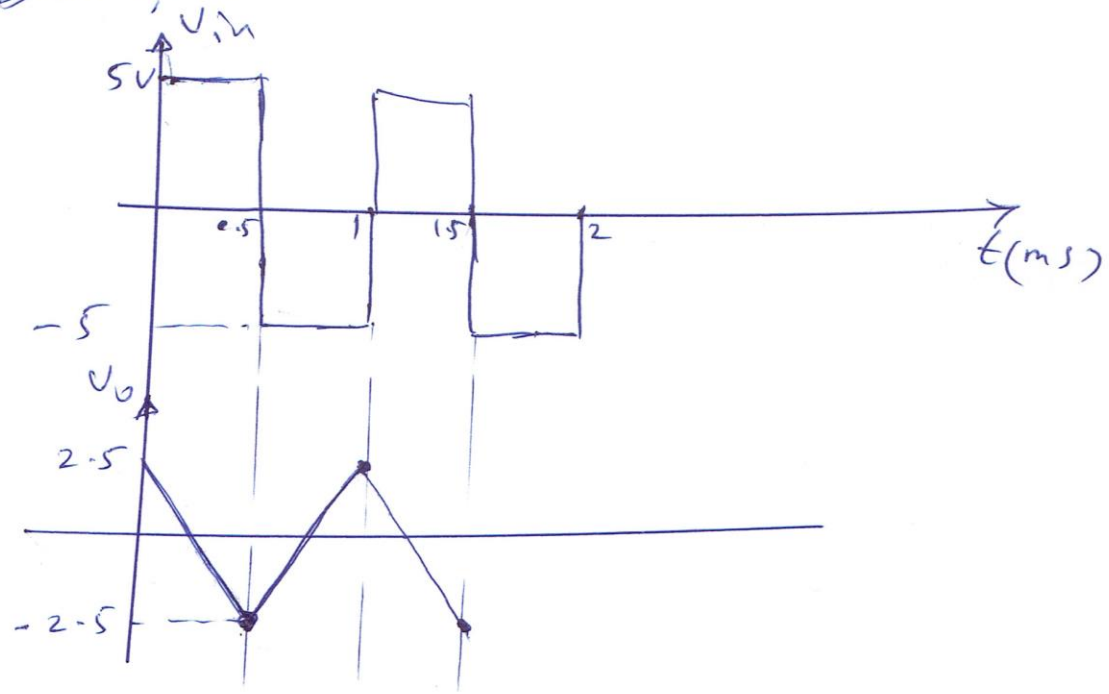
$= -2.5V$

[اي ان البولتية عند نهاية الجزء الموجب من الموجة تساوي (-2.5)]

* for negative half cycle, $V_{in} = -5$ Volt

$\therefore V_o = 2.5V$

[اي ان البولتية عند نهاية الجزء السالب من الموجة تساوي (2.5)]



(2)

ex(2): Draw the output voltage of the differentiator if the input voltage is given in Fig. a, and the freq. is 1KHz (R = 10K, C = 0.1Mf)

Solution:- $f = 1KHz \Rightarrow t = \frac{1}{1000} = 1ms$

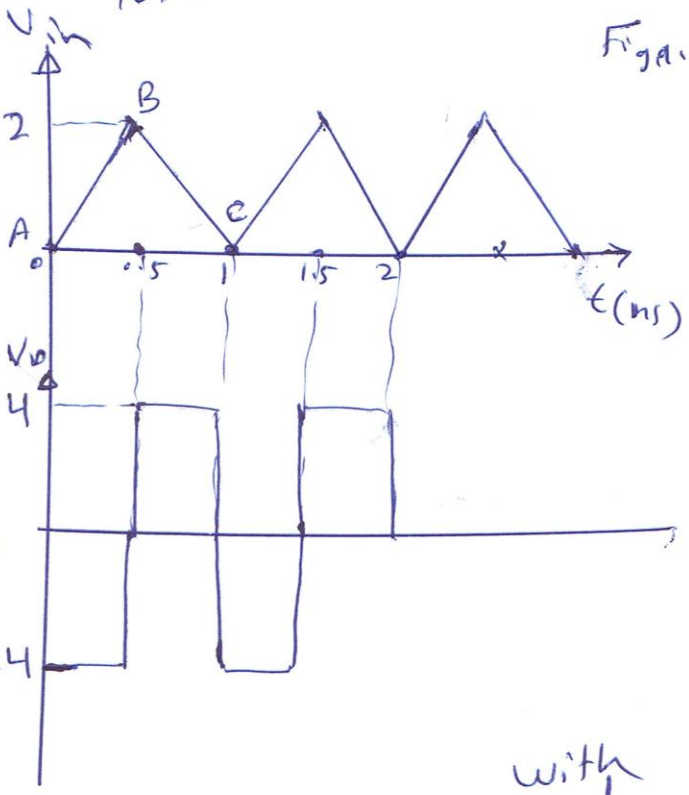


Fig a.

$A \rightarrow B$

$$\frac{dV_{in}}{dt} = \frac{\Delta V_{in}}{\Delta t} = \frac{2-0}{0.5-0} = 4 * 10^{3} V/s$$

$$V_o = -RC \frac{dV_{in}}{dt} = -10 * 10^{3} \times 0.1 * 10^{-6} \times 4 \times 10^{3}$$

$$= -4V$$

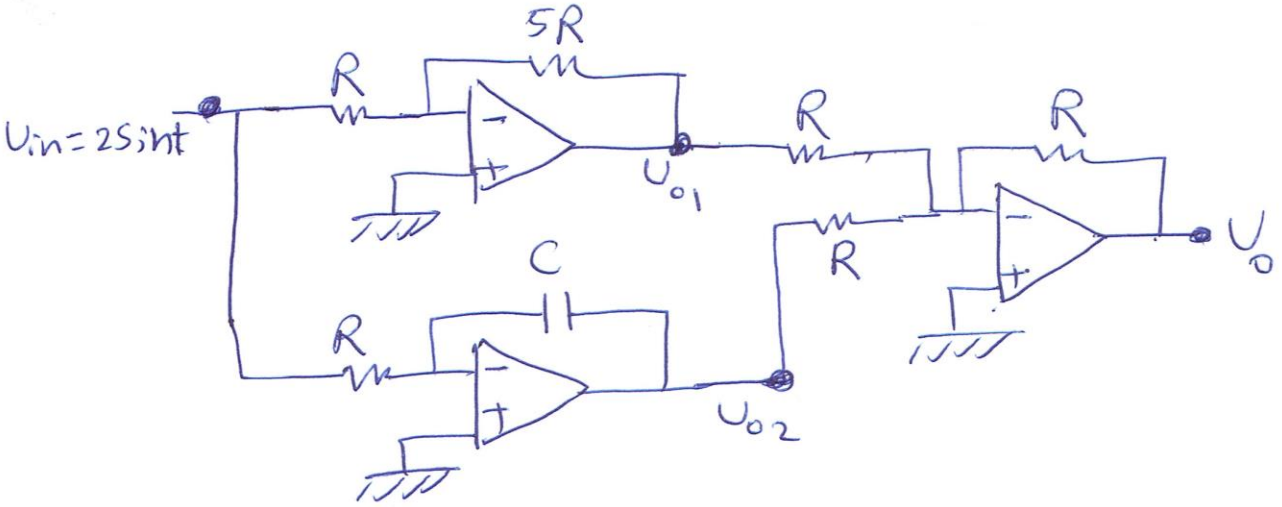
$B \rightarrow C$

$$\frac{dV_{in}}{dt} = \frac{\Delta V_{in}}{\Delta t} = \frac{0-2}{1-0.5} = -4 * 10^{3} V/s$$

$$V_o = 4V$$

This means that the output voltage is a square wave with $4V_p$ with the same freq. of the input voltage

ex(3) Design a circuit with help of op-amp that give output ($V_o = 10\sin t - 2\cos t$) if the input voltage is ($V_{in} = 2\sin t$). (assume $RC = 1$)

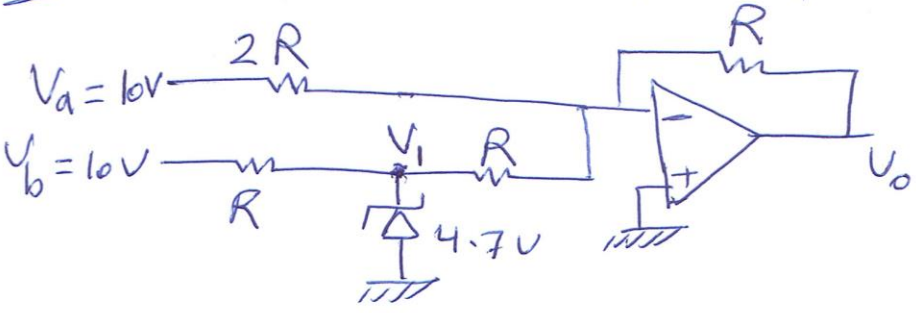


$$V_{o1} = \frac{-5R}{R} * 2\sin t = -10\sin t$$

$$V_{o2} = -\frac{1}{RC}\int V_{in}\,dt = -1\int 2\sin t\,dt = 2\cos t$$

$$V_o = -(V_{o1} + V_{o2}) = -(-10\sin t + 2\cos t) = \boxed{10\sin t - 2\cos t}$$

ex(4) :- what is the output of this circuit ($V_{sat} = \pm 13$)



Solution :- $V_1 = 4.7\ V$

$$V_o = -\left(\frac{R}{R}V_1 + \frac{R}{2R} \times 10\right) = -(4.7 + 5) = -9.7\ \text{Volt}$$

problem :- repeat ex. 4 if

① $V_b = 3$ volt

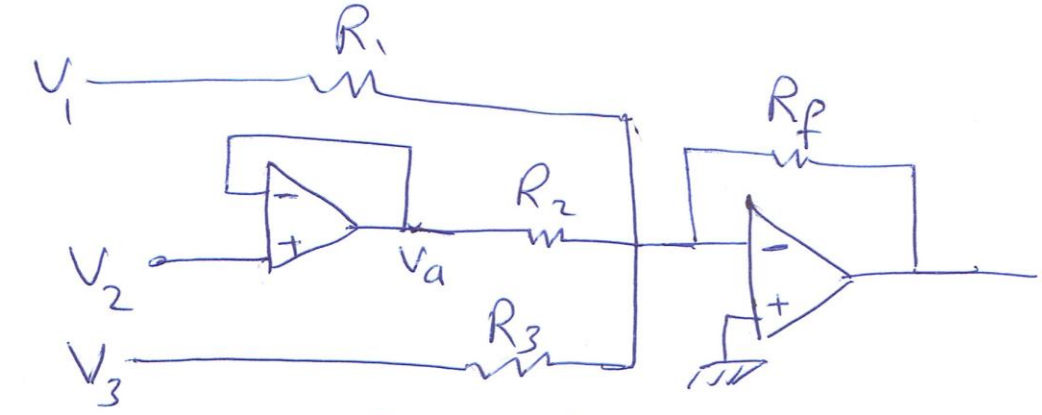
② all resistances have the same values (with $V_b = 10$)

③ Zener diode is reversed ~~($V_b = 3$ V)~~ ($V_b = 3V$)

---

ex 5 :- for the circuit shown in figs, find the relation of the output voltage

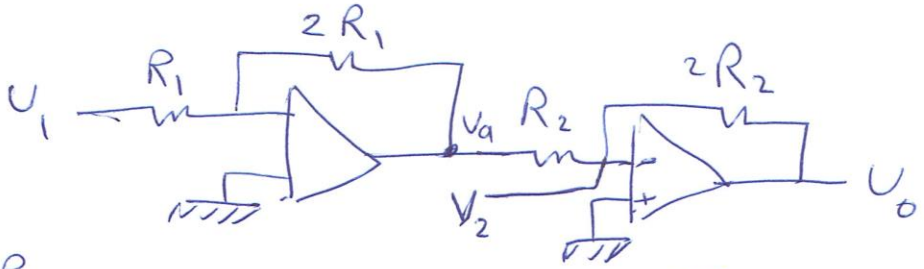
①



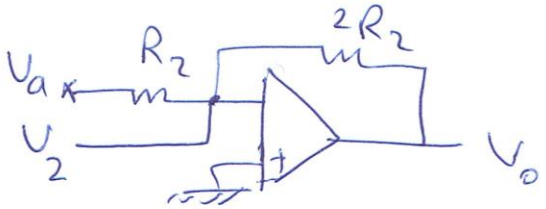
$U_a = U_2$ (voltage follower)

$$U_o = -\left(\frac{R_f}{R_1}U_1 + \frac{R_f}{R_2}V_2 + \frac{R_f}{R_3}U_3\right)$$

②



$$U_a = -\frac{2R_1}{R_1}U_1 = -2U_1$$



$$\frac{V_a - V_2}{R_2} = \frac{V_2 - V_o}{2R_2} \Rightarrow V_a - V_2 = 0.5V_2 - 0.5V_o \Rightarrow 0.5V_o = 1.5V_2 - V_a$$

$$\therefore V_o = 3V_2 - 2V_a \Rightarrow \boxed{V_o = 3V_2 + 4V_1}$$

(5)

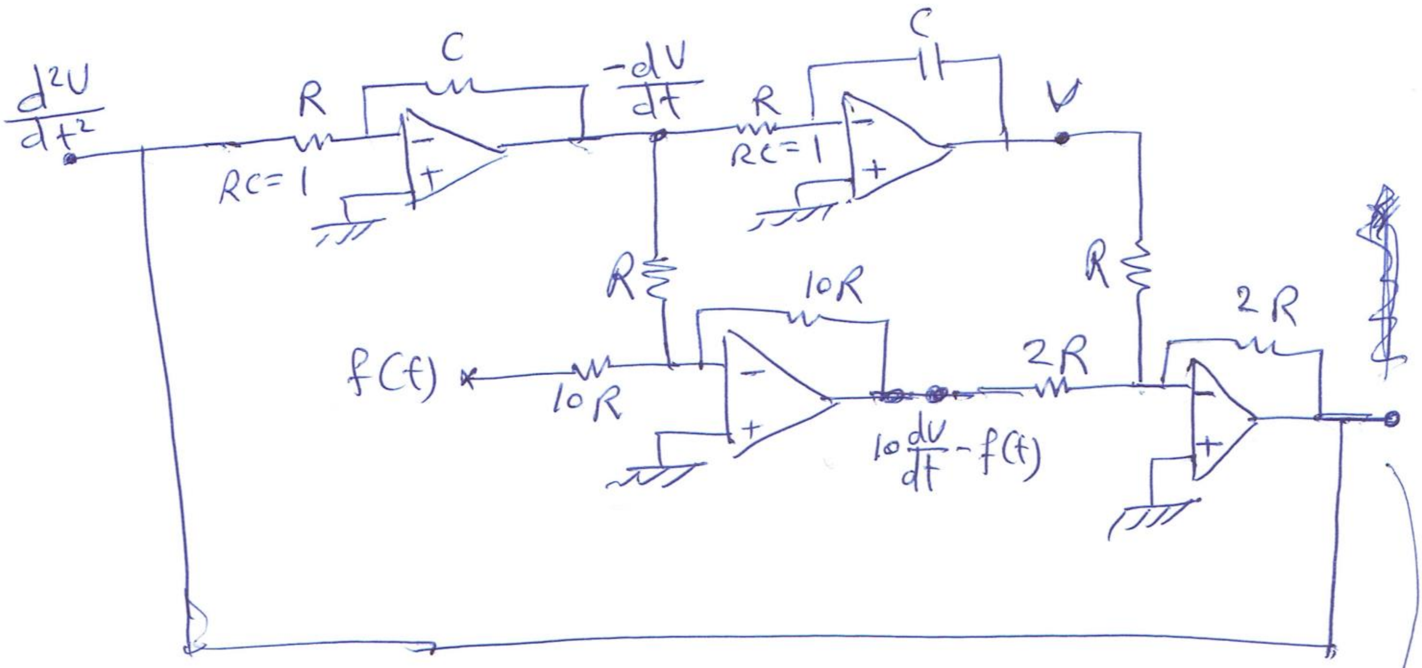
ex 6 Desigen Circuit to solve the following differential equation

$$f(t) = \frac{d^2V}{dt^2} + 10\frac{dV}{dt} + 2V$$

Solution

ترتيب المعادلة بحيث تكون أعلى مشتقة بالطرف الأيسر

$$\frac{d^2V}{dt^2} = -10\frac{dV}{dt} - 2V + f(t)$$



في مثل هذه الأسئلة نأخذ أعلى مشتقة ونجعلها
هي (i/p) وفي هذا المثال ($\frac{d^2V}{dt^2}$) وعند تكاملها
نحصل على ($\frac{dV}{dt}$) وعند تكاملها مرة أخرى
نحصل على (V) ، وبإضافة هذه الحدود الى
الدالة [f(t)] نحصل على ($\frac{d^2V}{dt^2}$)
والذي نقيده بمسار تغذية عكسية الى نقطة البداية

$$\frac{d^2V}{dt^2} = -10\frac{dV}{dt} - 2V + f(t)$$

Digital to Analog conversion

It is an important interface process for converting digital signals to analog signals. An example is a voice signal that is digitized for storage, processing, or transmission and must be changed back into an approximation of the original audio signal in order to drive a speaker.

The *R*/2*R* ladder is more commonly method used for D/A conversion because it requires only two resistor values as shown in Fig. 48 for four bits.

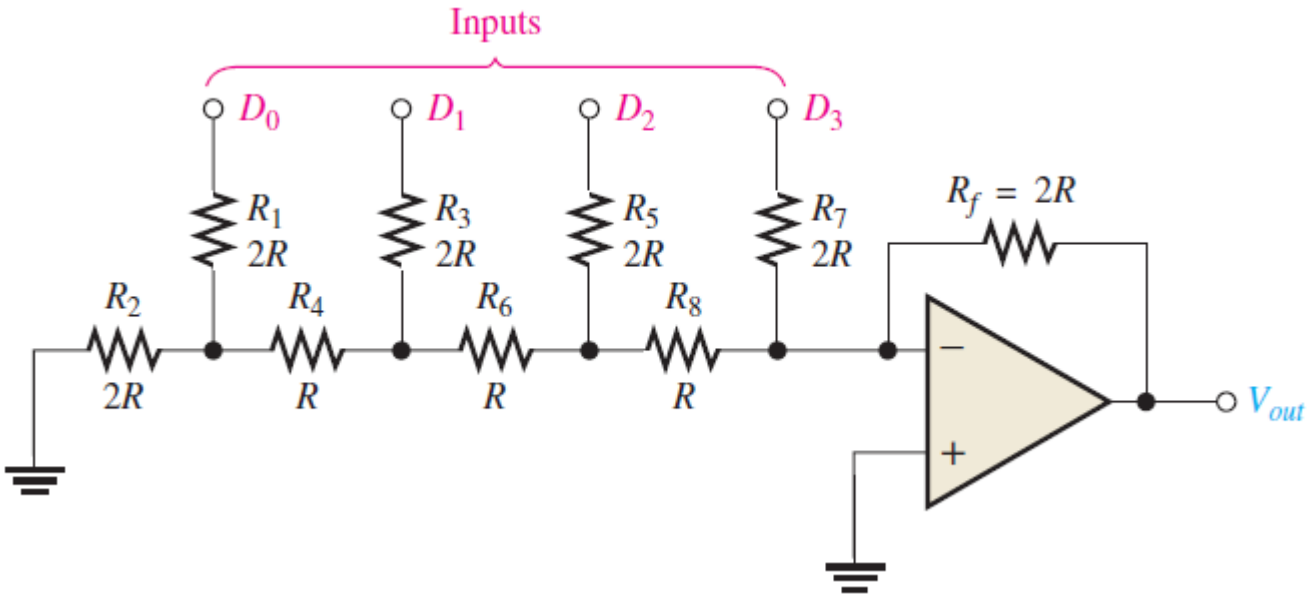
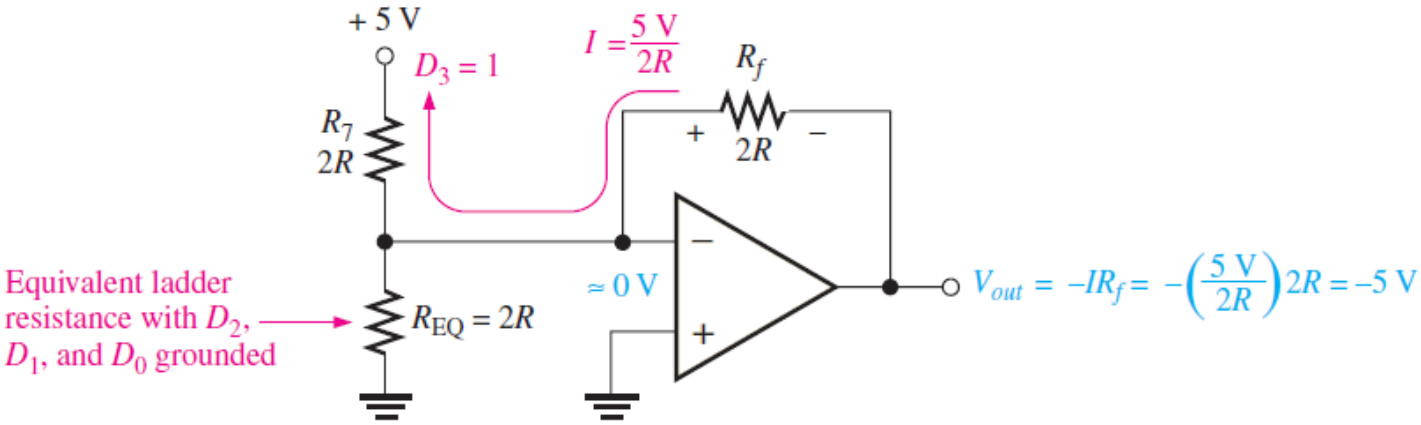


Fig. 48

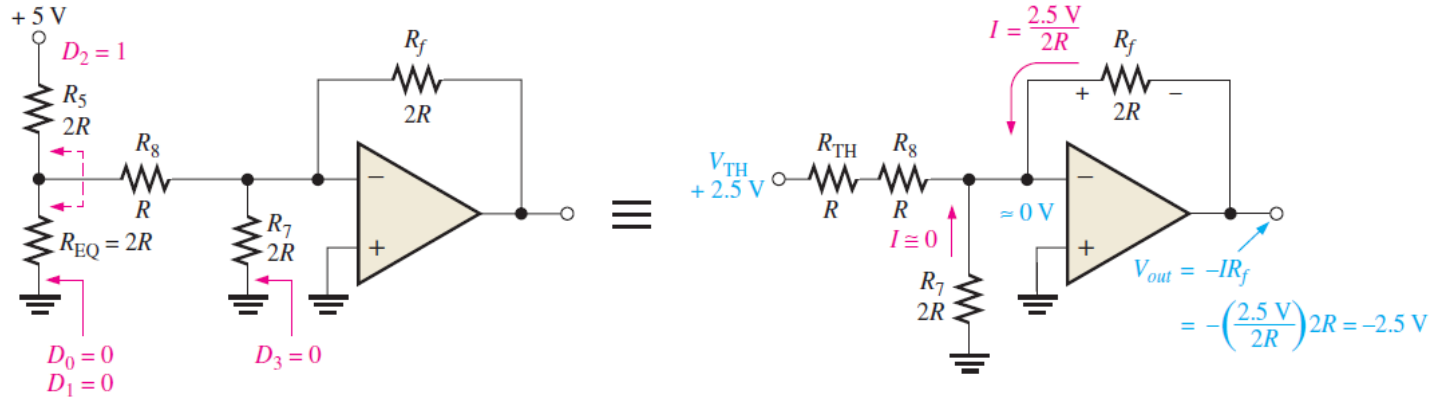
Assume that the *D*3 input is HIGH (+5 V) and the others are LOW (ground, 0 V). This condition represents the binary number 1000. A circuit analysis will show that this reduces to the equivalent form shown in Fig. 49 (a).

Essentially no current goes through the 2*R* equivalent resistance (R_{EQ}) because the inverting input is at virtual ground. Thus, all of the current (I=5/2R) through *R*7 is also through *Rf*, and the output voltage is -5V.



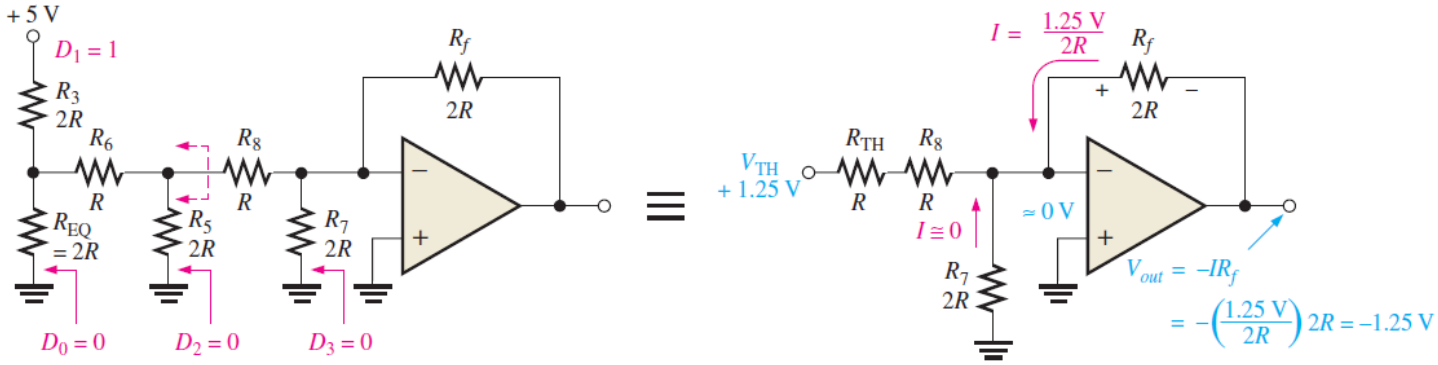
(a) Equivalent circuit for $D_3 = 1$, $D_2 = 0$, $D_1 = 0$, $D_0 = 0$

Figure (b) shows the equivalent circuit when the *D*2 input is at +5 V and the others are at ground. This condition represents 0100. If we thevenize looking from *R*8, we get 2.5 V in series with *R*, as shown. This results in a current through *Rf* of *I*= 2.5/2*R*, which gives an output voltage of -2.5V. Keep in mind that there is no current from the op-amp inverting input and that there is no current through *R*7 because it has 0 V across it, due to the virtual ground.



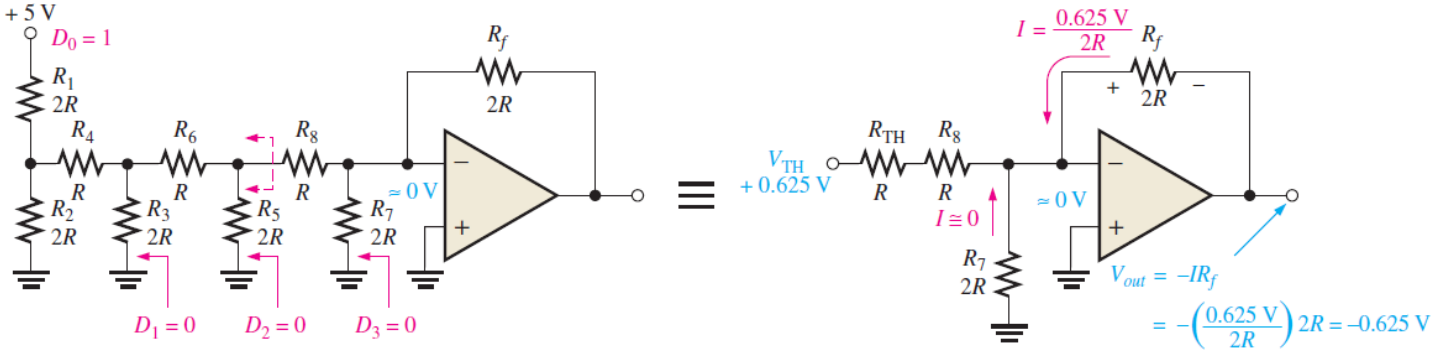
(b) Equivalent circuit for $D_3 = 0$, $D_2 = 1$, $D_1 = 0$, $D_0 = 0$

Figure (c) shows the equivalent circuit when the *D*1 input is at +5 V and the others are at ground. This condition represents 0010. Again thevenizing looking from *R*8, you get 1.25 V in series with *R* as shown. This results in a current through *Rf* of *I*= 1.25 V/2*R*, which gives an output voltage of -1.25.



(c) Equivalent circuit for $D_3 = 0$, $D_2 = 0$, $D_1 = 1$, $D_0 = 0$

In Fig. (d), the equivalent circuit representing the case where *D*0 is at +5 V and the other inputs are at ground is shown. This condition represents 0001. Thevenizing from *R*8 gives an equivalent of 0.625 V in series with *R* as shown. The resulting current through *Rf* is *I*=0.625V/2*R*, which gives an output voltage of -0.625 V.



(d) Equivalent circuit for $D_3 = 0$, $D_2 = 0$, $D_1 = 0$, $D_0 = 1$

Notice that each successively lower-weighted input produces an output voltage that is halved, so that the output voltage is proportional to the binary weight of the input bits.

In summary, We can prove that the equivalent analog voltage shown in Fig. 50 below is obtained from the relation:

$$V_{analog} = \frac{V_A + 2V_B + 4V_C + 8V_D + \ldots}{2^n}$$

((The proof is left as an exercise))

Where (n) is the number of digital inputs.

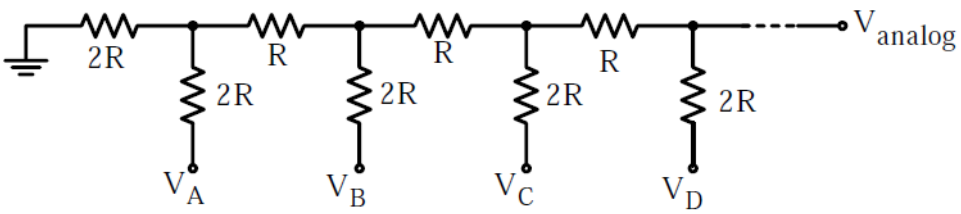


Fig.50

Figure 51 shows a four−bit R−2R ladder network and an op−amp connected to form a DAC. The op amp shown is an inverting amplifier and in this case the reference voltage (V_{ref}) should be negative so that the amplifier output will be positive. Alternately, a non−inverting op amp could be used with a positive value of (V_{ref})

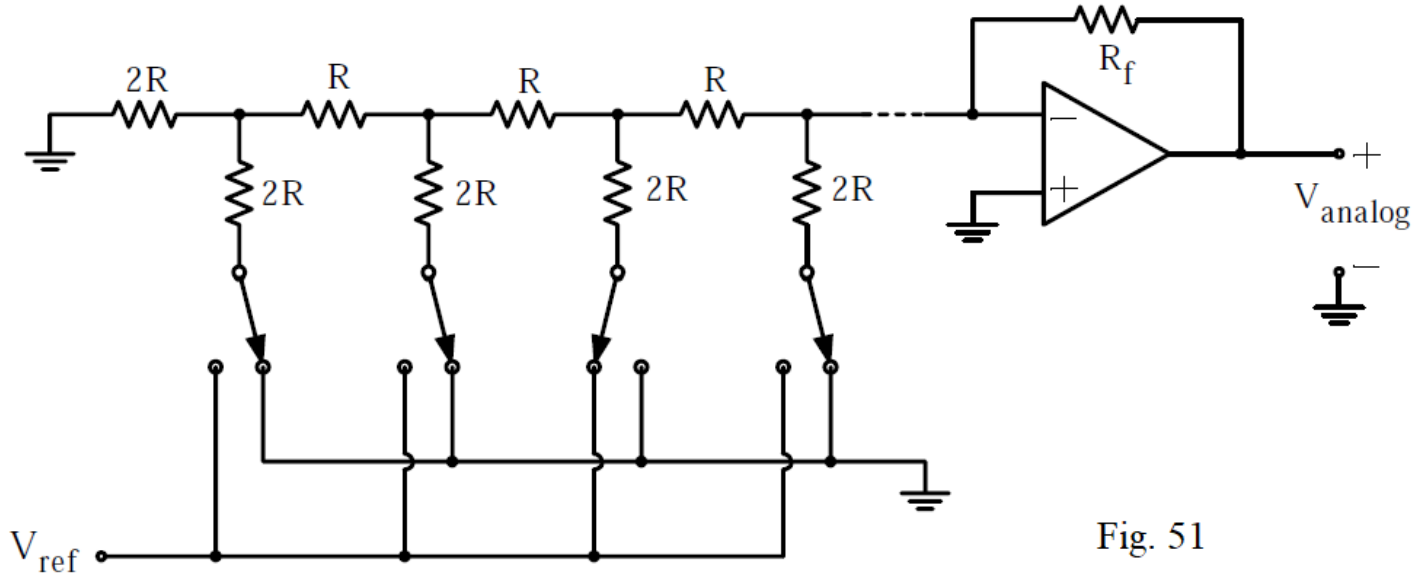


Fig. 51

Example: Figure 52 shows a four−bit DAC where all four switches are set at the ground level. Find the analog voltage value at the output of the unity gain amplifier for each of the sets of the switch positions shown in Table. Fill−in the right−most column with your answers.

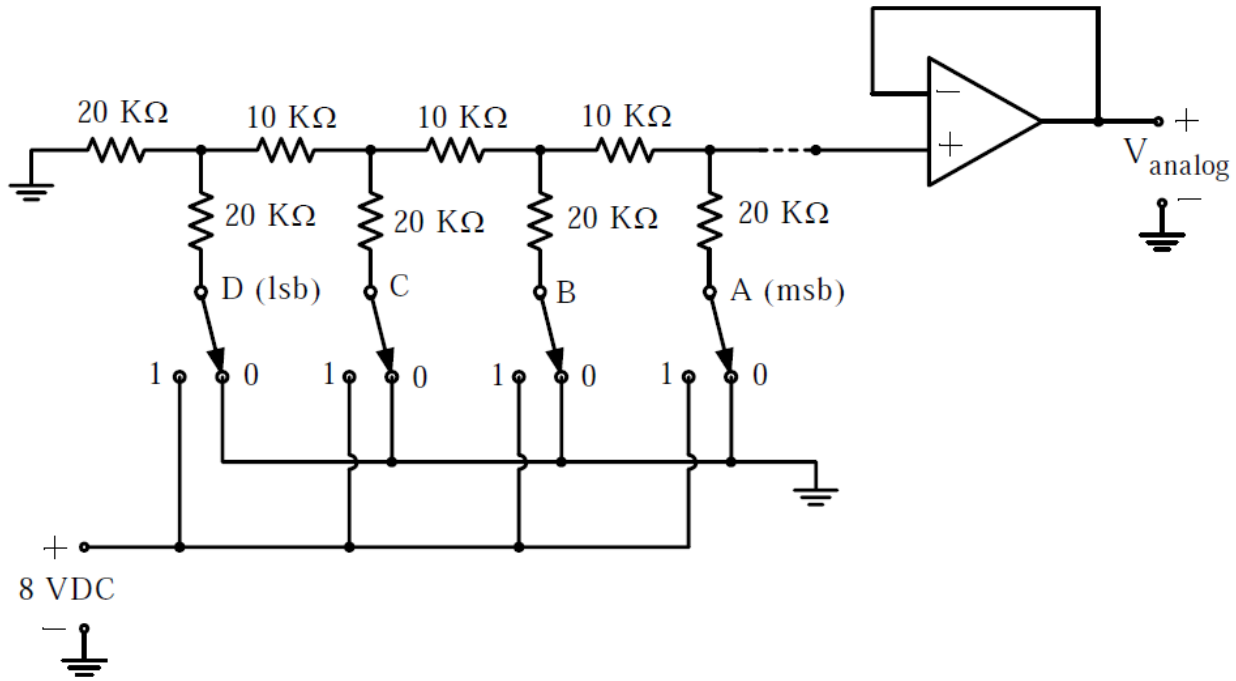


Fig. 52

	A 2^0	B 2^1	C 2^2	D 2^3	
(a)	1	1	1	1	
(b)	1	0	0	1	
(c)	1	0	1	0	
(d)	0	1	0	0	

Solution:

This is a 4−bit DAC and thus we have $n=2^4=16$ distinct binary values from 0000 to 1111 corresponding to decimals 0 through 15 respectively.

a. $$V_{analog} = \frac{V_A + 2V_B + 4V_C + 8V_D}{2^n} = \frac{1\times 8 + 2\times 8 + 4\times 8 + 8\times 8}{2^4} = 7.5\ V$$

b. $$V_{analog} = \frac{V_A + 2V_B + 4V_C + 8V_D}{2^n} = \frac{1\times 8 + 2\times 0 + 4\times 0 + 8\times 8}{2^4} = 4.5\ V$$

c. $$V_{analog} = \frac{V_A + 2V_B + 4V_C + 8V_D}{2^n} = \frac{1\times 8 + 2\times 0 + 4\times 8 + 8\times 0}{2^4} = 2.5\ V$$

d. $$V_{analog} = \frac{V_A + 2V_B + 4V_C + 8V_D}{2^n} = \frac{1\times 0 + 2\times 8 + 4\times 0 + 8\times 0}{2^4} = 1.0\ V$$

Based on these results, we can now fill−in the right−most column with the values we obtained, and we can plot the output versus inputs of the R−2R network for the voltage levels and as shown in Figure 53.

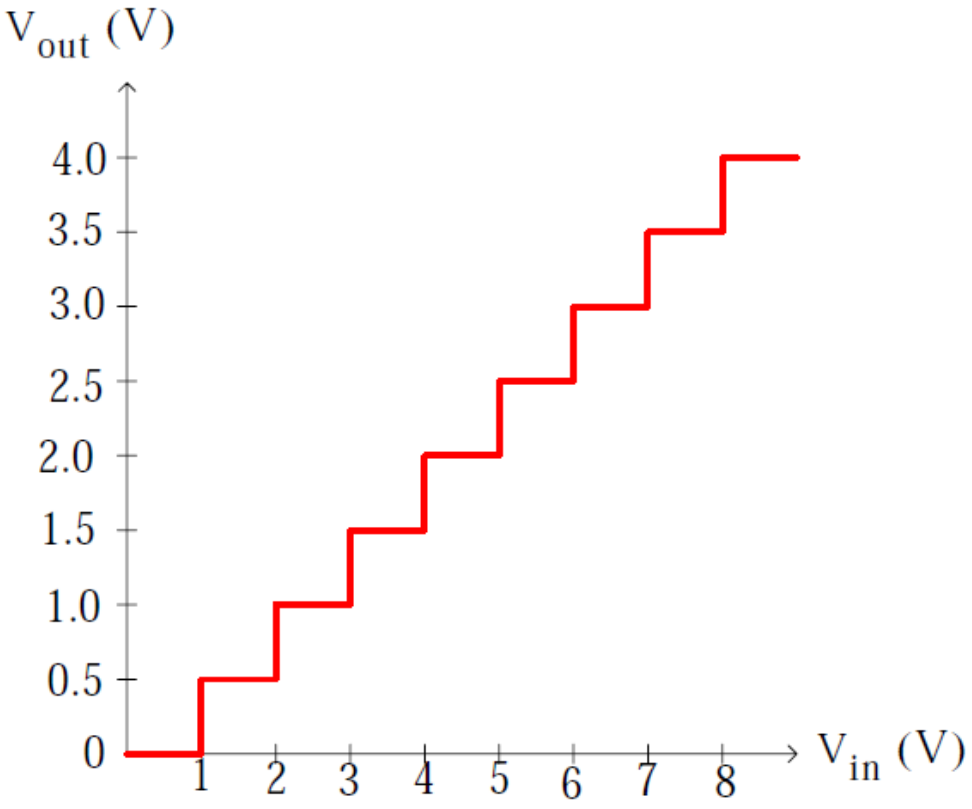


Fig.53

Active Filters

A filter circuit can be constructed using passive components like resistors and capacitors. But an active filter, in addition to the passive components makes use of an *OP-AMP* as an amplifier. The amplifier in the active filter circuit may provide voltage amplification and signal isolation or buffering. There are four major types of filters namely, low-pass filter, high-pass filter, and band-pass filter and band-stop filter. All these four types of filters are discussed in the following sections.

1- ***low−pass filter*** transmits (passes) all frequencies from dc or zero frequency up to a *critical* (*cutoff*) frequency denoted as w_c, and *attenuates* (blocks) all frequencies above this cutoff frequency. An op amp low−pass filter is shown in Figure 54(a &b) and its amplitude frequency response in Figure 54(c).

In Figure 54(c), the blue lines represent the ideal characteristics and the smooth curve represents the practical characteristics, where the gain does not reduce immediately to zero. The vertical scale represents the magnitude of the ratio of output to input voltage V_{out}/V_{in}, that is, the gain A_v.

The cutoff frequency w_c is the frequency at which the maximum value of V_{out}/V_{in} falls to $0.707C_v$, and this is called the *half power* or the -3dB point.

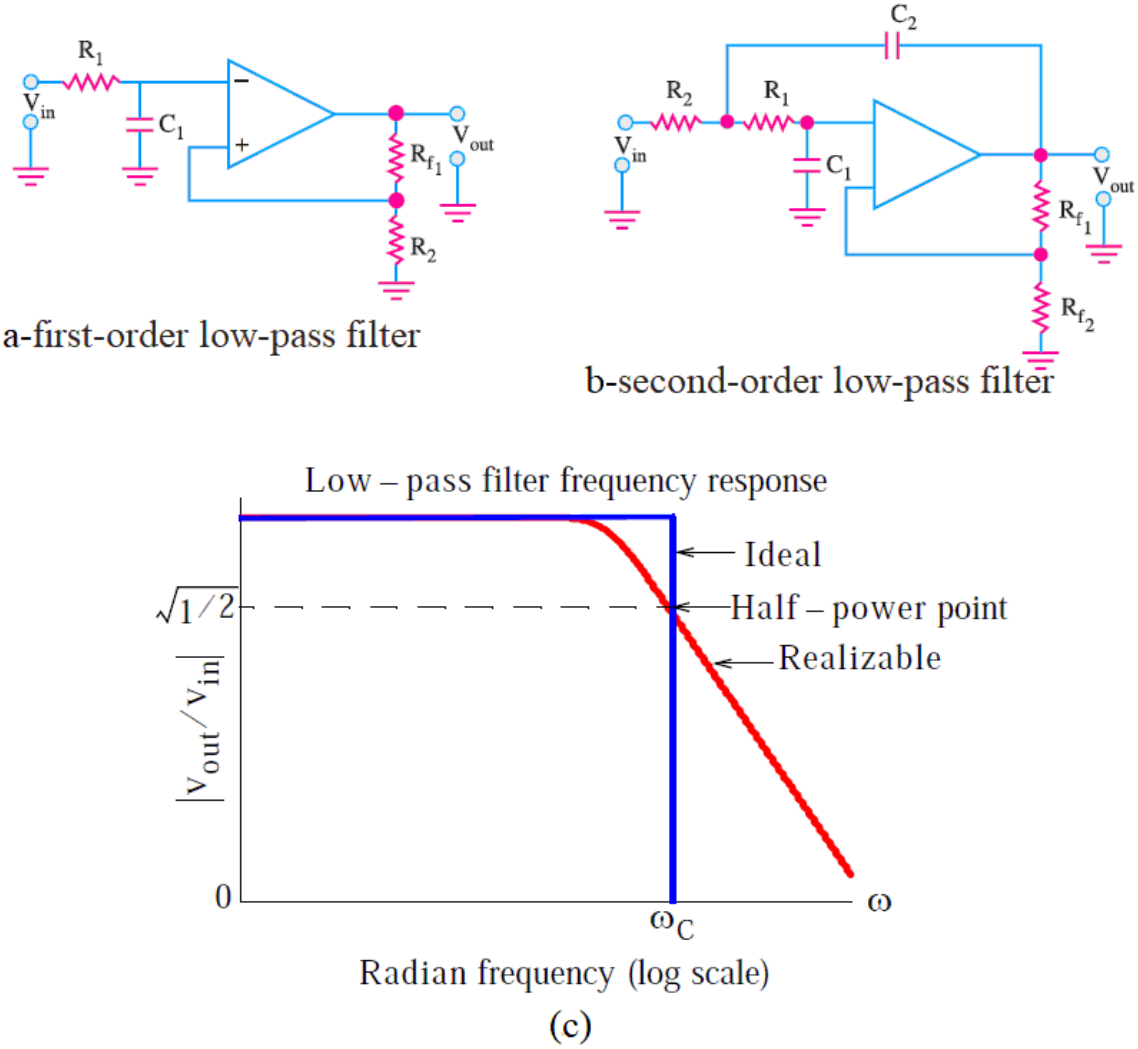
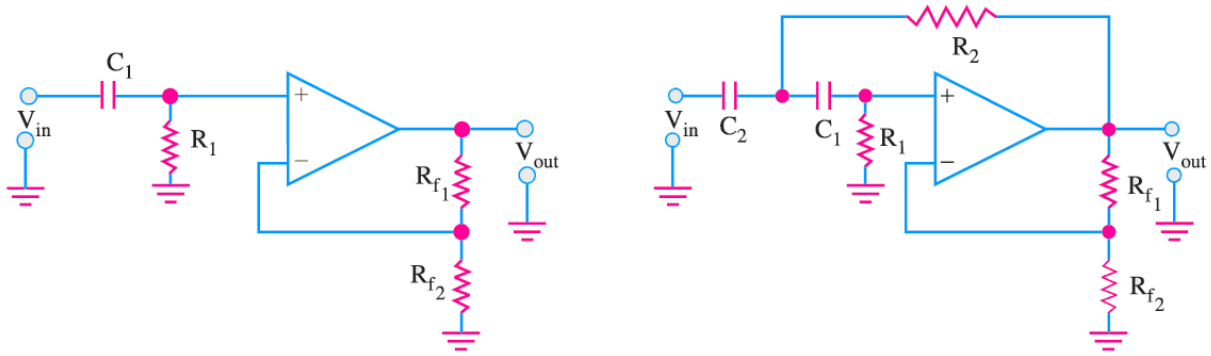
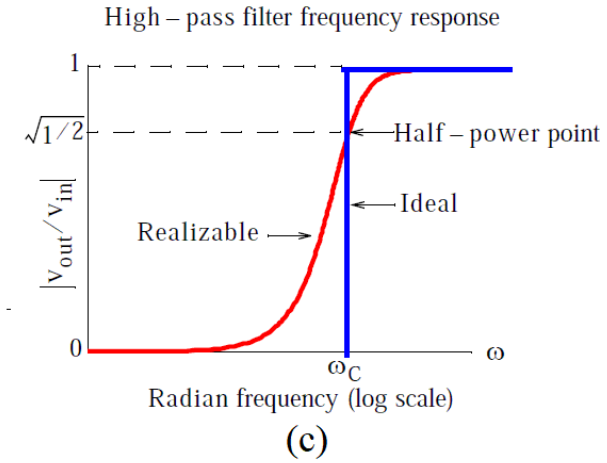


Figure 5 4. An active low−pass filter and its amplitude frequency response

2- ***high−pass filter*** passes all frequencies above a cutoff frequency w_c , and blocks all frequencies below the cutoff frequency. An op amp high−pass filter is shown in Figure 55(a&b) and its frequency response in Figure 55(c).



(*a*) first order high-pass filter (*b*) second-order high-pass filter.



(c)

Figure 5 5. An active high–pass filter and its amplitude frequency response

3- ***band–pass* filter** passes the band (range) of frequencies between the cutoff frequencies denoted as w_1 and w_2, where the maximum value of A_v which is unity, falls to $0.707C_v$, while it blocks all frequencies outside this band. A simple way to construct a band-pass filter is to cascade a low-pass filters and a high-pass filter as shown in Figure 56(a) and its frequency response in Figure 56(b). The values of w_1 and w_2 can be obtained by using the relations, $1/R_1C_1$ and, $1/ R_2 C_2$. Then band width,

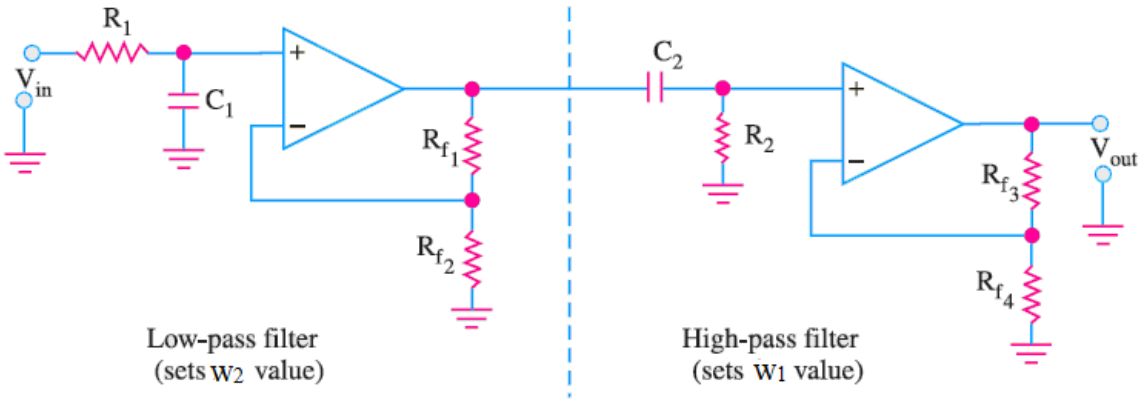
$$BW = w_2 - w_1$$

And the centre frequency,

$W_0=w_1w_2$

The Quality-factor (or *Q*-factor) of the band pass filter circuit.

Q=W0/BW



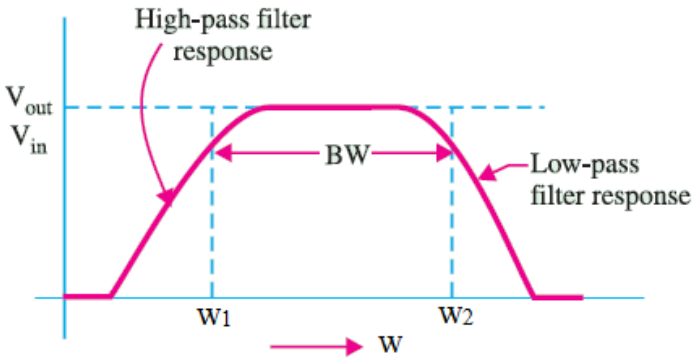
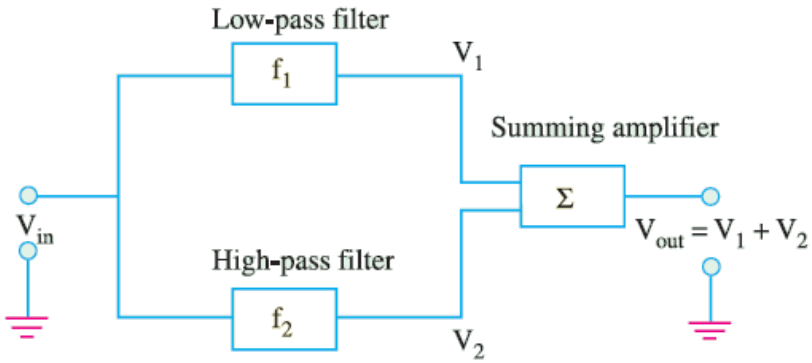
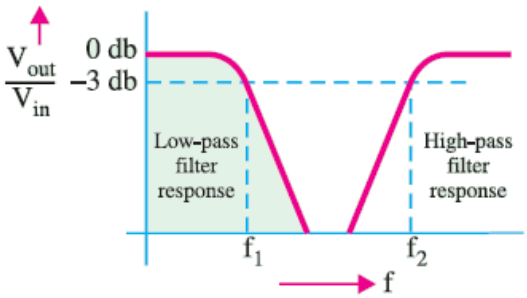


Fig 56

4- ***band−elimination*** **or** ***band−stop*** **or** ***band−rejection*** **filter** attenuates (rejects) the band of frequencies between the critical (cutoff) frequencies denoted as w_1 and w_2, where the maximum value of C_v which is unity, falls to $0.707C_v$, while it passes all frequencies outside this band. An op amp band−stop filter is shown in Figure 57(a) and its frequency response in Figure 57(b).
The block diagram shows that the circuit is made up of a high-pass filter, a low-pass filter and a summing amplifier. The summing amplifier produces an output that is equal to a sum of the filter output voltages. The circuit is designed in such a way so that the cut-off frequency, *w*1 (which is set by a low-pass filter) is lower in value than the cut-off frequency, *w*2 (which is set by high-pass filter). The gap between the values of *w*1 and *w*2 is the bandwidth of the filter.
When the circuit input frequency is lower than *w*1, the input signal will pass through low-pass filter to the summing amplifier. Since the input frequency is below the cut-off frequency of the high pass filter, V2 will be zero. Thus the output from the summing amplifier will equal the output from the low-pass filter. When the circuit input frequency is higher than *w*2, the input signal will pass through the high-pass filter to the summing amplifier. Since the input frequency is above the cut-off frequency of the low-pass filter, V1 will zero. Now the summing amplifier output will equal the output from the high-pass filter.



(*a*)



(*b*)

Butterworth Filter

There are many different types of active filters. Among the most useful of them are Butterworth filters because they have an excellent response. Butterworth filters, named after British engineer Stephen Butterworth.

Table-1 below gives the Butterworth polynomials for n up to 8. Note that for n even, the polynomials are the products of quadratic forms, and for n odd, there is present the additional factors (s+1).

NORMALIZED POLYNOMIALS THAT PRODUCE BUTTERWORTH RESPONSES

ORDER	NORMALIZED DENOMINATOR POLYNOMIALS
1	$(s+1)$
2	$(s^2+1.414s+1)$
3	$(s+1)(s^2+s+1)$
4	$(s^2+0.7654s+1)(s^2+1.848s+1)$
5	$(s+1)(s^2+0.6180s+1)(s^2+1.618s+1)$
6	$(s^2+0.5176s+1)(s^2+1.414s+1)(s^2+1.932s+1)$
7	$(s+1)(s^2+0.445s+1)(s^2+1.247s+1)(s^2+1.802s+1)$
8	$(s^2+0.390s+1)(s^2+1.111s+1)(s^2+1.663s+1)(s^2+1.962s+1)$

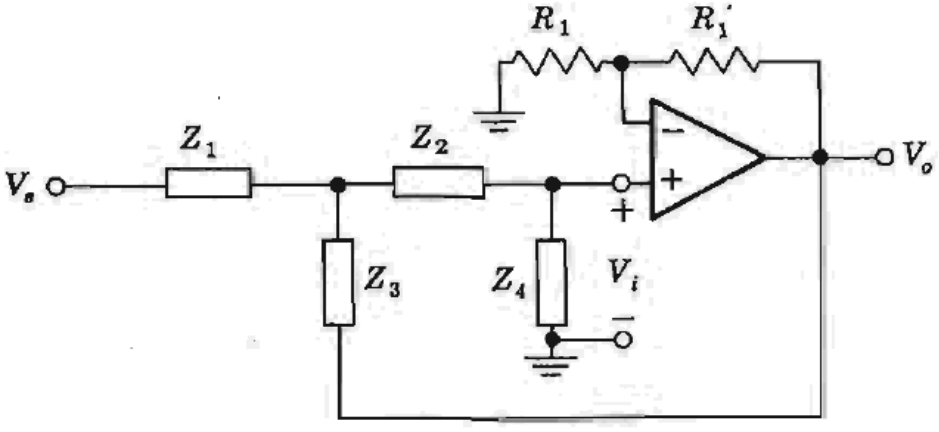
$$2k = 3 - A_{Vo} \quad \text{or} \quad A_{Vo} = 3 - 2k \qquad \text{.....(1)}$$

And

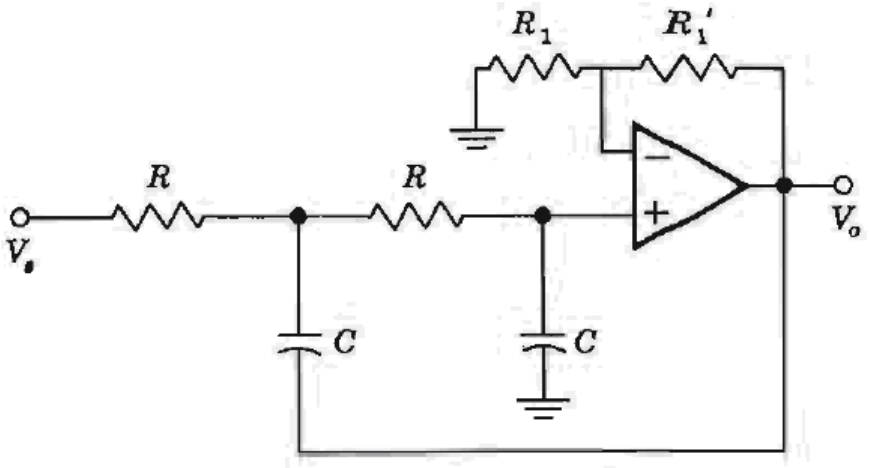
$$\omega_o = \frac{1}{RC}$$

We are now in a position to synthesize even-order Butterworth filters by cascading prototypes of the form shown in Fig. b , using identical R's and C's and selecting the gain A_{Vo} of each operational amplifier to satisfy Eq. (1) and the damping factors from Table 1.

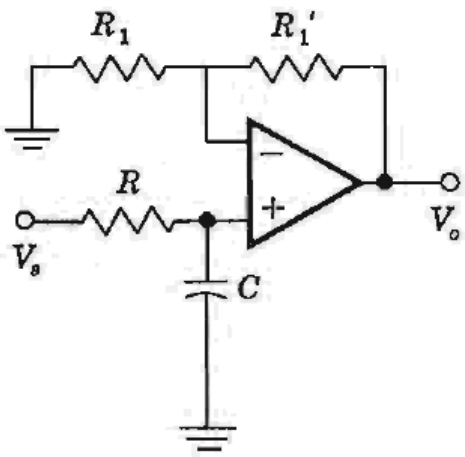
To realize odd-order filters, it is necessary to cascade the first-order filter of Eq. (1) with second-order sections such as indicated in Fig. b . The first-order prototype of Fig. c has the transfer function of Eq. (1) for arbitrary A_{Vo} provided that ω_o is given by Eq. (2) . For example, a third-order Butterworth active filter consists of the circuit in Fig. b in cascade with the circuit of Fig. c, with R and C chosen so that $RC = 1/\omega_o$



(a) Generalized active-filter prototype.



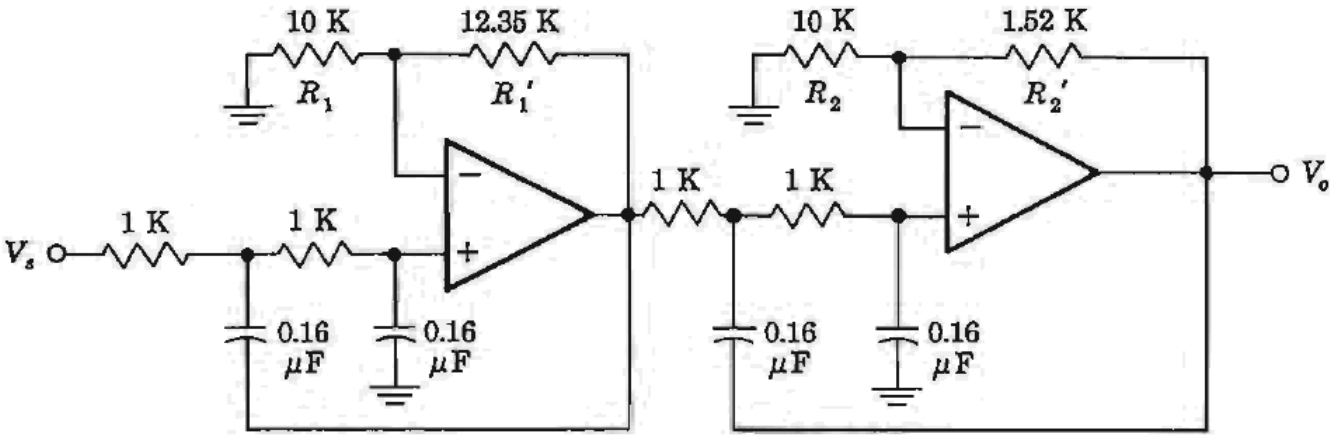
(b) Second-order low-pass section.



(c) First-order low-pass section.

Example: design a fourth-order Butterworth low-pass filter with a cutoff frequency of 1kHz.
Solution
we cascaded two second-order prototypes as given below.

Item	First Stage	Second Stage
Stage parameters	$K_1 = 0.7654$ $f_0 = 1000$ k	$K_2 = 1.848$ $f_0 = 1000$ k
Design constraints and Element values	Av1=3-2k1=2.235 Av1= (R1+$\bar{R}$1)/R1 Choose R1= 10k ➔ $\bar{R}$1=12.35 k f_0=1/2πRC ➔ let R=1k ➔ C=0.16uF	Av2=3-2k2=1.152 Av_2= (R2+$\bar{R}$2)/R2 Choose R2= 10k ➔ $\bar{R}_2$= 1.52k f_0=1/2πRC ➔ let R=1k ➔ C=0.16uF



designs Final

Exercise: design a third-order Butterworth low-pass filter with a cutoff frequency of 10kHz.