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DESIGN AND SIMULATION OF OPTICAL LOGIC GATES BASED ON DIFFRENT PLASMONIC WAVEGUIDES FOR OPTICAL COMMUNICATIONS

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(M. Sc. In Communications Techniques Eng.)

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DESIGN AND SIMULATION OF OPTICAL LOGIC GATES BASED ON DIFFRENT PLASMONIC WAVEGUIDES FOR OPTICAL COMMUNICATIONS

THESIS

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BY

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2021

بِسْمِ اللَّهِ الرَّحْمَنِ الرَّحِيمِ

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We certify that this thesis titled " **Design and Simulation of Optical Logic Gates Based on Different Plasmonic Waveguides for Optical Communications**" which is being submitted by Wissam Abed Jasim was prepared under my/our supervision at the Communication Techniques Engineering Department, Engineering Technical College-Najaf, AL-Furat Al-Awsat Technical University, as a partial fulfillment of the requirements for the of of Technical Master degree in Communication Engineering.

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Committee Report

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Abstract

Photonics is considered a better solution to speed up data transmission than electronics; however, there is still the issue of signal dispersion when the size of the optical components is reduced in integrated optical circuits. The plasmonic technology plasmonic waveguides (PWs) came as a solution for this problem, where the electromagnetic waves are confined to the metal - insulator or insulator – metal surface. Thus they will fill in the gaps of electronics (large bandwidth and high speed) and photonics (overcoming diffraction due to reduced size). In the current work, two structures are suggested, the first uses an insulator - metal – insulator (IMI) PWs and the second uses a metal - insulator – metal (MIM) PWs. Hence, all photo-plasmonic gates were proposed, analysed, designed, and simulated using the COMSOL MULTIPHSECSE 5.5. The first proposed structure uses (IMI) PWs. The second proposed structure uses a (MIM) PWs . Each of the two structures has five gates (OR, NOR, AND, NAND and NOT), and the working principle of these gates is based on the features of constructive and destructive interference that occurs between the input and control signals. The transmission threshold selected is 0.25% for both structures to implement these five gates. The implementation of these gates is of the same structure, the same dimensions, and the same wavelength is 1550 nm for all the proposed plasmonic logic gates in the same structure. The transmission in some plasmonic logic gates in both structures exceeded 100%. For example, the OR gate had transmission of 124% in the first structure using the IMI PWs and the transmission in the OR gate is 121% in the second structure using the MIM PWs. Each structure had a relatively small area of (300×350)nm for the first structure that used the IMI PWs and the area is (650×750)nm for the second structure that used the MIM PWs.

It was noticed from the simulation results that the structure dimensions are less when using the IMI PWs type.

Acknowledgment

In the name of God, the Most Gracious, the Most Merciful. Praise be to God for His guidance throughout this work, and blessings and peace be upon His Prophet Muhammad and his honorable family. First, I would like to dedicate this work to my master and mentor, the Commander of the Faithful, Ali Ibn Abi Talib, peace be upon him, and the Awaited Imam Muhammad al-Mahdi, peace be upon him.

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I would also like to thank my family, especially my wife, who gave me a lot of support, encouragement and love. Without them, this work would not have seen the light of today.

Declaration

I hereby declare that the work in this thesis my own except for quotations and summaries which have been duly acknowledged.

December 15, 2021 Wissam Abed Jasim Alehtari

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List of Abbreviation

Abbreviation	Description
2-D	Two Dimensions
3-D	Three Dimensions
ALU	Arithmetic Logic Unit
CMOS	Complementary Metal Oxide Semiconductor
CPML	Convolutional Perfectly Matched Layer
C.R	Contrast ratio
DMD	Dielectric-Metal-Dielectric
DWs	Dialectic Waveguides
EM	Electromagnetic
FDTD	Finite Difference Time Domain
FEM	Finite Element Method
FoM	Figure of Merit
ICs	Integrated Circuits
IMI	Insulator-Metal-Insulator
LRSPPs	Long-Range Surface Plasmon Polaritons
MIM	Metal-Insulator-Metal
MDM	Metal-Dielectric-Metal
MZI	Mach–Zehnder Interferometer
PWs	Plasmonic Waveguide
Q-factor	Quality Factor
SOI	Silicon-On-Insulator
SPP	Surface Plasmon Polariton

SPPs	Surface Plasmon Polaritons
SRSPPs	Short-Range Surface Plasmon Polaritons
TM	Transverse Magnetic

List of Symbols

Symbol	Definition
R	Resistance of conductor
ρ	Electric resistivity
ε_0	Permittivity of free space
ε_d	Permittivity of dielectric material
L	Length of conductor
l	Length of plate
W	Width of conductor
w	Width of plate
T	Thickness of conductor
d	Distance between plates
C	Capacitance
β	Propagation Constant
k_x	The Wave number for x-direction
k_y	The Wave number for y-direction
k_z	The Wave number for z-direction
ε_c	Permittivity of core material
ω	Angular frequency
c	Speed of light
n_c	Core refractive index
λ_0	Wavelength in vacuum
d_x	Fundamental mode size in x-direction
d_y	Fundamental mode size in y-direction

ε_m	Permittivity of metal
K	Wave number
k_d	Dielectric wave number
k_m	Metal wave number
k_0	Free space wave number
d	Metal and dielectric thickness
n_{eff}	Effective refractive index
L+	Anti-symmetric mode
L-	Symmetric mode
F	Gate function
Q	Output of the logic gate
X1	First input of all logic gates
X2	Second input of all logic gates
$\overline{X1}$	Complement first input
Ls	Length of the side stripes
h	height of stripes
a	Inner rib of Nano-squire ring
b	Outer rib of Nano-squire ring
d	Coupling distance between stripes and Nano-squire rings
h_c	Height of the slot cavity
w_c	width of the slot cavity
g	The coupling distance between the ports and the slot cavity
w	The width of the waveguide port

Δl	The distance between the ports and the center of the slot cavity
λ_{spp}	Surface plasmon polariton resonance wavelength
m	Mode number
ε_x	Electric field component of TM mode (x-component)
ε_y	Electric field component of TM mode (y-component)
T	Transmission
P_{out}	Output optical power
P_{in}	Input optical power for single port
$P_{out}\|\mathrm{ON}$	Output optical power in ON state
$P_{out}\|\mathrm{OFF}$	Output optical power in OFF state
m	Interference order
λ_{inc}	Incident wavelength
θ	Phase of incident wave
L_{spp}	Propagation length for surface plasmon polariton

Chapter1

General Introduction

1. 1 Introduction

Over the past few years, the rate and speed of data transmission and bandwidth have been of significant concern of researchers of communications. The optical signal processing method has been used to boost these parameters. This method is based on directing the optical signal in the waveguides. Several studies have been conducted to examine the applications of the optical waveguides, especially in optical communication systems, optical systems and integrated optical circuits. These optical devices in optical signal processing applications have many advantages such as high data transmission rate, large bandwidth, to overcome the problem of scattering, resistance to outer interference, which means high security, and low energy consumption. Hence, in recent years all optical devices have been based on Surface Plasmon Polaritons (SPPs) a large scale plasmonic technology. This technology has the potential to overcome the scattering that occurs in traditional waveguides and the delays and heat that is typical of electronic devices. Plasmonic devices are also called sub-wavelength devices, because in these devices we can manipulate the sub-wavelength scale [1, 2]. SPPs are the interaction of electromagnetic waves and free electrons in metals and propagate between the interface of metal - insulator or insulator - metal [3] producing collective waves in which billions of electrons vibrate in sync at optical frequencies. SPPs waves can propagate through nanoscale wires. Many studies were proposed on nano-optical devices have been attained, such as resonators [4], nano cavities [5], dividers [6], couplers [7], modulators [8], demultiplexers [9], waveguides [10], Hybrid plasmonic waveguides [11], switches [12], and logic gates [13]. In the

field of optical gates, many studies have been conducted as well, such as, hybrid plasmonic photonic crystals and nano-slot cavities [14], silicon waveguides [15], silicon nano ring resonators [16]. Recently, several structures of plasmonic optical devices such as nanoscale logic gates have been proposed [17]. This thesis introduces two structures and each structure consists of five optical plasmonic logic gates (OR, NOR, AND, NAND and NOT). These gates are carried out in the first structure using the IMI PWs and in the second structure the MIM PWs is used. The applicable wavelength for both structures is 1550 nm. The first structure was designed using a square nano-dual resonator and a linear waveguide as for the second structure, is designed using a slot-cavity- resonator and linear waveguides (MIM). The simulation was implemented at the gates of both structures using COMSOL MULTIPHYSICS (5.5), to obtain the results in the both structures was the Finite Element Method (FEMs), as it is expected that these devices will be a gateway for implementing integrated optical plasmonic circuits in the future.

1.2 Problem statement

1-There is one issue overlooked. It concerns what happens to the dimensions of the structure when the structure itself executes a number of optical plasmonic gates which operate utilizing the same wavelength and the same transmission threshold for all gates executed within the same structure when using one type of the plasmonic waveguides. This issue also concerns what happens at the case of building another structure which executes the same number of the optical plasmonic gates operating via the same wavelength and the same transmission threshold while the using a different type of the plasmonic waveguide.

2- The number of the executed logic gates in the existent structures is small. In addition, the dimensions of these structures are big in size.

1.3 Research Objectives

1- Proposing two structures, each implementing the same number and type of plasmonic logic gates, where each structure uses a different type of plasmonic waveguide. The first structure uses the (IMI) PWs while the second structure uses the (MIM) PWs.

2- Implementing the largest number of gates in a single structure; five logic gates (OR, AND, NOR, NAND and NOT) with the same structural dimensions, the same resonant frequency, the same wavelength, and the same transmission threshold.

1.4 General Methodology

To achieve the aim of this study, the methodology explicated in the chart is shown below:

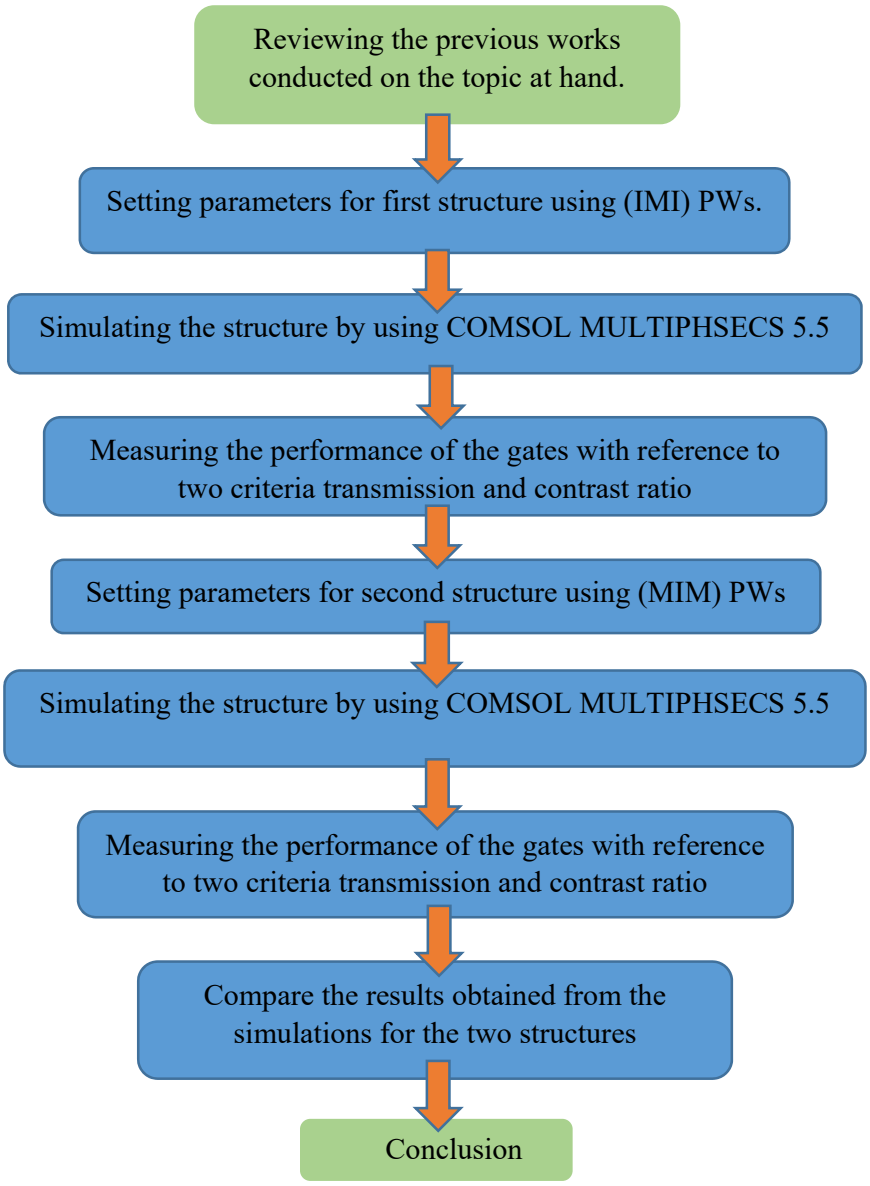


Figure 1.1: General Methodology

1.5 Research Contribution

The current study achieved the following contributions:

1. According to the researcher's knowledge, there is no two structures of small size are proposed to implement five gates in one structure, with the same resonant frequency and wavelength and the same transmission threshold. Hence, in this study, one structure is adopted to implement the largest number of logical functions (five gates) which leads to reduction in the cost of (manufacturing, time, dimensions and shape).

2. In the two prospective structures, an IMI PWs in the first structure and MIM PWs in the second structure are used. The results of simulations are compared. Accordingly, transmission exceeded 100% in some gates for both structures, such as OR gate in (IMI) PWs and OR and AND gate in (MIM) PWs.

3. It is unprecedented to achieve a wavelength of 1550 nm and to be used in both structures as it is considered the best option in optical communication systems, which creates easy compatibility in the two structures with optical communication systems in the future.

1.6 Structure of the Thesis

The current thesis is divided into five chapters. Each chapter begins with an introduction that highlights the main topics of the chapter. The following is a brief overview of the remainder of the thesis:

Chapter Two presents a detailed review of the plasmonic technology in addition to the principles under which this technology operates, the advantages and disadvantages of this technology, the basic properties of (Surface Plasmon Polaritons (SPPs), as well

as the applications of plasmonics, plasmonic waveguides, and the principle of traditional logic gates.

Chapter Three is dedicated to explain the simulation of the first structure to implement five optical-plasma logic gates using a (IMI) PWs that works on the basis of constructive and destructive interference. All five gates were implemented with the same structure, the same dimensions, the same resonance frequency and the same wavelength and transmission threshold. The simulation results were presented, discussed and the performance of these five implemented logic gates were measured, depending on two criteria: transmission and contrast ratio.

In Chapter Four, the simulation of the second structure was explained to implement five photo-plasmonic logic gates using a (MIM) PWs that works on the basis of constructive and destructive interference. All five gates were implemented with the same structure, the same dimensions, the same resonance frequency and the same wavelength and transmission threshold. The simulation results were presented, discussed and the performance of these five implemented logic gates were measured, depending on two criteria: transmission and contrast ratio.

In Chapter Five, the concluding remarks of the results obtained in the previous two chapters discussed, and suggestions given for future work to achieve the best results.

Chapter 2

Theoretical Background and Literature Survey

2.1 Introduction

This chapter introduces definitions of the plasmonic technology and it presents a brief history of this technology. Later, the chapter presents the electronic and Photonics limitations that conflict with reducing devices to nanometer size. Next, the chapter outlines the advantages and disadvantages of the plasmonic technique. After that, an explanation is provided regarding the theoretical principles of plasmonic technology. This is followed by a description concerning the basic properties of Surface Plasmon Polaritons (SPPs). Following, an explanation for the plasmonic waveguides is presented including the properties of the SPPs that exist between the multiple layers of the two types (IMI) PWs and (MIM) PWs. Then, the chapter explains the comparison between the two types of waveguides. Also, the applications of plasmonics are explained. In addition to that, it surveys the principle of traditional logic gates. Also, previous works that are closely related to this current study will be presented. Finally, the chapter presents a definition of performance-evaluating parameters used in comparing types of plasmonic waveguides.

2.2 Definition and History of Plasmonics

Long before the research began on Plasmonic technology, it had been used by German artists to decorate antiques and glass handicrafts to create different colors in their artworks. Golden and silver nanoparticles of different sizes and shapes were used on the glass to form attractive colors on those antiques, such as the famous Lycurgus Cup

in the 4th century (AD) as shown in Figure 2.1. The cup appears green when exposed to external light as shown in Figure 2.1.a and appears red when exposed to internal light as shown in Figure 2.1.b. Also, when the light falls on it tangentially on the other corner, it can appear in other colors as shown in Figure 2.1.c where the electromagnetic field (EM) oscillates with the oscillation of the incident light on the free electrons of metals [18].

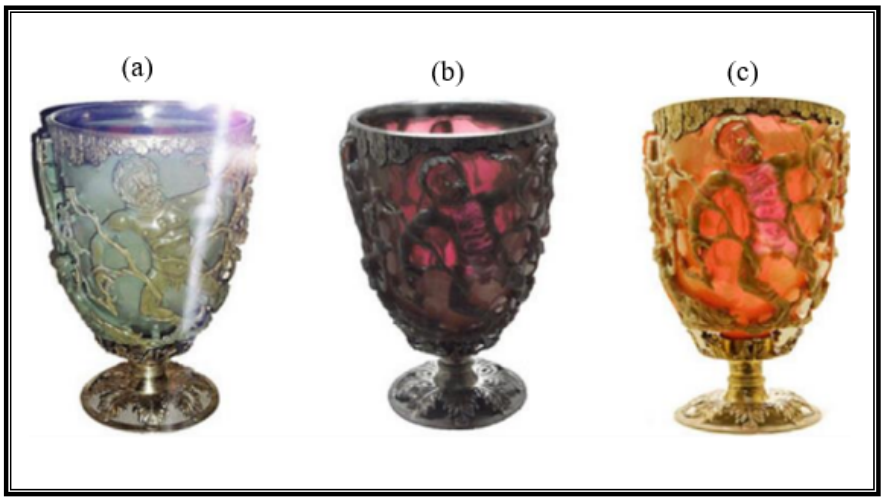


Figure 2.1 Lycurgus cup (a) when exposed to external light and (b) when exposed to internal light and (c) when the light falls on it tangentially on the other corner [18].

Richie first described surface plasmon polaritons in 1957 (SPPs) who theoretically investigated the low-energy plasma loss spectra of electrons moving through the thin metal [19]. Thus, the term "Plasmonic" is derived from (electronic plasma), but the term refers to the applications of Plasmonics, which is the study of the branch of optoelectronics/nano-engineering. It studies how the electromagnetic field (EM) can be confined to dimensions smaller than the wavelength of the incident electromagnetic signal (which is why it is called the sub-wavelength technique). Hence, it is a new interesting field, integrating the powers of electronics and photonics together. The

development of nanofabrication techniques helps increase the applications of nanostructures. [20] Plasmonic is a quasiparticle or collective excitation in which billions of electrons oscillate in synchrony at optical frequencies resulting from a force exchange of energy between an electromagnetic wave and an excitation in a material for instance, photon-electron coupling. When the electromagnetic waves fall on a metal- insulator or insulator- metal interface as shown in Figure 2.2, the electrons will accelerate and lead to polarization, resulting in recovering the force that causes the free electron oscillation of the metal as shown in Figure 2.3. This oscillation is quantized and the oscillation of free electrons is quantized plasma oscillations and is called SPP. [21] In this case, electromagnetic surface waves are excited and propagated along the interface Figure 2.4 [22]. These surface waves are continually transient in the vertical direction and are known as surface Plasmon Polaritons (SPPs). [23] SPP metallic waveguides are nanostructures that initiates the possibility to confine and guide light waves at the nanometer scale [24].

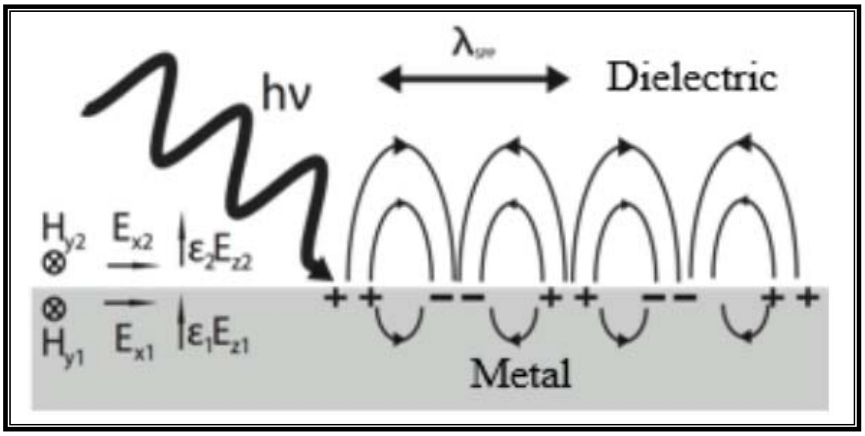


Figure 2.2 Incident Electromagnetic Wave on a insulator-Metal Interface [25]

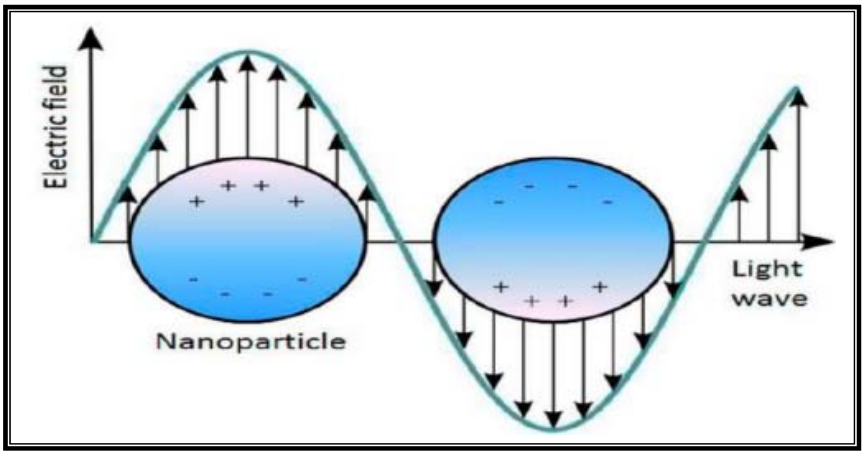


Figure 2.3 Schematic describing surface plasmon resonance of metallic nanoparticle [26]

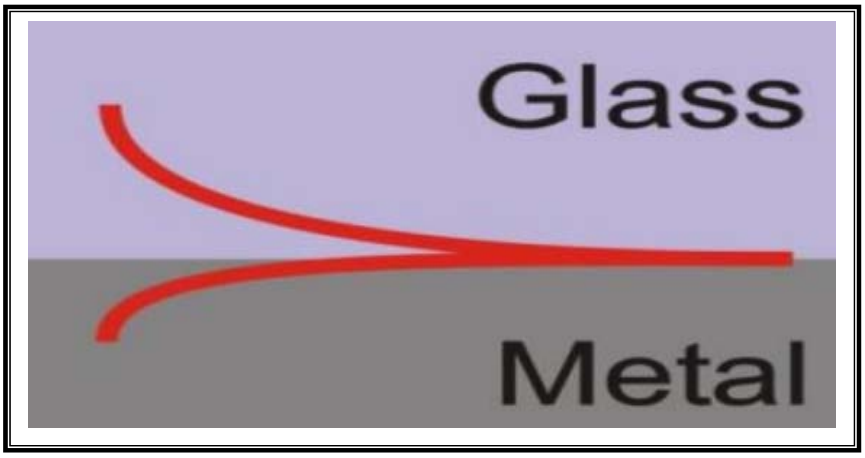


Figure 2.4 Propagation of Surface Plasmon Polariton (SPP) waves [27]

2.3 The Importance of Plasmonic

2.3.1 Electronic Limitations

It has become necessary in communication systems to demand an increase in information transmission and faster data processing due to the constant need for faster, smaller and more efficient devices. Therefore, the trend of electronic devices has recently moved towards nanoscale production of ultra-fast transistors, such as Intel microprocessor [28-29]. The main component of integrated circuits (ICs) are the connections that are connected together to distributes electrical signals and energy to other components in the (IC). After size reduction of the components to the nanoscale, IC performance becomes highly dependent on the connections unlike a transistor where its functions improve by decreasing size, and the efficiency of interconnection decreases, which limits the speed of digital circuits and electronic devices [30] because the connections are made of copper material. Hence, when their size is reduced to the nanometer scale, the delays will increase due to the increase in effective resistance, capacitance, interference and radiation [31- 32]. Furthermore, the time constant affects the connection line, due to the resistance and capacitance of the line [33]. It is clear from the resistance and capacitance given in equations (2.1) and (2.2) respectively, that the smaller the conductor size, the greater its resistance [33].

$$R = \frac{\rho L}{W\,T} \tag{2.1}$$

$$C = \frac{\varepsilon_0 \varepsilon_d l\, w}{d} \tag{2.2}$$

where ρ is the electrical resistance, ε_o and ε_d are the permittivity of free space and the dielectric material, respectively. L and l are the lengths of the conductor and the plate, respectively. W and w are widths of the conductor and the plate, respectively. T and d

are a thickness of the conductor and the distance between the plates, respectively. It is clearly shown by the above equations that when the interconnection is scaled down to the nanoscale, R increases because of the inverse proportional relationship with W, and C increases due to the decrease in d. Therefore, copper connections are limited by bandwidth and capacity. Thus, this will limit a number of components that can be placed on a chip. Because electronics deals with a flow of the charges (electrons) as the frequency increases (electronic pulse), the electronic device becomes heated and the wires become very loose. Thus, high-frequency transmission or high data transmission becomes impossible, i.e, a huge amount of data cannot be transferred. Moreover, the second obstacle is when a size of the electronic wires decreases and the resistance increases. This will cause a time delay. Instead of using a chip with single-core processor, multi- core processor are used to boost the performance [34]. However, such chips are reduced in size to nanometers and the number of cores and wires increases. Connecting these cores leads to an increase in the connections and it occupies a large area of the chip. Moreover, a large part of the energy is lost in the connecting wires, which leads to the loss. This especially happens in low-power devices. It is therefore known that there are limits to the extent to which cores are placed. On the other hand, the basic building blocks of the Arithmetic Logic Unit (ALU) are logic gates. These logic gates operate badly due to the low speed of the transition between logic 0 and logic 1 in electronics. Thus an alternate method should be used especially when speed and data rate are very high. However, an optical integrated circuit could solve this problem significantly, which can deal with the function of each on the as an optical component such as, dielectric photonic connections due to their compatibility with complementary metal oxide semiconductor (CMOS) electronics [34-35]. Optical interfaces offer various solutions to the

limitations mentioned in electronics. These connections give high bandwidth and low-loss interconnection between optics and electronics [36], which results in better processing to the distributed components and cores, better operating performance, higher speed and bandwidth, and lower losses than those of electronic connections.

2.3.2 Photonics Limitations

Photonics is the study of optics and electronics. It includes all types of manipulation of light, such as generation, emission, transmission, modulation, amplification and detection [37]. The dielectric optical connectors have high speed, wide bandwidth and low energy consumption compared to electronic connectors. Nevertheless, optical connectors are 1000 times more expensive than their electronic counterparts [38]. When it was necessary to reduce the size of large optical devices to micro devices in the sub-micrometer and nanometer range in order to take advantage of their high capacity. The miniature optical devices are often used for their ability to withstand capacity 1000 times greater than electronic circuits [39-40-41]. The optical networks have been established with a wide range of digital signals in communications. The scalability of these networks has revolutionized the next generation of integrated optical communications on the chip [32]. The progress in modern technology has led to an improvement and simplicity in the techniques of manufacturing optical devices. A number of silicon-on-insulator (SOI) devices were proposed for high-density optical integrated circuits. This is due to the high refractive index contrast as well as the excellent optical properties at frequencies of optical fibers in communications [32] as well as the Mach-electro-optical modulator Match-Zehnder which is a type of SOI device. This optical device converts the electrical signal into an optical signal, by encoding a light wave with a high-speed electronic signal. Optical (modulators) rates

of up to 10 Gbps have been demonstrated with low power consumption [32]. A grating coupler has been proposed using conventional (SOI) [42]. This device has coupling loss less than 1 dB, and easy integration into optical circuits [32]. Also, another device is the filter ring resonator that uses optical wires [43] which were experimentally tested and manufactured for more clarification [44]. The type of coupling resonance is indicated by the polarization separator. It uses photonic crystals using the effect of optical bandgap and micro-cavities. It is difficult to design a waveguide using optical crystals due to its small size and high contrast factor. Moreover, these crystals have very large losses compared to optical wires [45]. The signal connections represent a challenge that limits the speed in digital systems. However, the size is not identical between nanoscale electronic circuits and optical devices, as they have electronic and optical limitations for integration [46-47]. When the dimensions of the optical components are close to half the wavelength of light, optical dispersion will occur. This limits the propagation of light and limits the scalability and dimensions of optical devices [47-48-49] because there are three dimensions' 3D. The nature of the waves propagating in the insulator material is derived from equation (2.3).

$$\beta^2 + K_x^2 + K_y^2 = \varepsilon_c \frac{\omega^2}{c^2} \tag{2.3}$$

where β is the propagation constant k_x and k_y are the wave number in the x and y direction, respectively, ε_c is the dielectric constant of the core material,ω is the angular frequency for incident wave and c is the speed of light which is $3\times 10^8\ m/sec$ for a 3D wave propagation in an insulating waveguide with dielectric constant $\varepsilon_c > 0$, propagation constant $\beta = k_z$, both phase-shift constants k_x and $k_y$are real, this results in the upper bound on k_x and k_y is

$$k_x \, and \, k_y \leq (\omega/c)\sqrt{\varepsilon_c} = \frac{2\pi n_c}{\lambda_0} \tag{2.4}$$

where n_c is the refractive index of the core and λ_o is the wavelength of the vacuum. Through the upper bound, a lower bound is established in accordance with the size of the fundamental mode of wave propagation that depends on equation (2.4) [50]

$$d_x, d_y \geq \left(\lambda_0/2n_c\right) \tag{2.5}$$

where d_x and d_y are the size of the basic mode of wave propagation in the **x** and **y** direction respectively. This makes dielectric optical components one or two times larger than their electronic counterparts. Moreover, optical devices are frequency dependent and have a narrow bandwidth depending on the configuration of the device and the limitation of its use and efficiency, because these limitations are a result of scattering phenomenon of the use of optical devices with a size smaller than the operating order. This phenomenon results in a lot of power dissipation and therefore it is not possible to send a large amount of data with miniaturization. Thus, the process of miniaturization to the nanometer scale of the optical device is ineffective and impossible in practice, especially when the optical device that operates in a frequency band in terahertz, i.e. (λ is greater than 1000 nanometers). Therefore, it is necessary to find a technology or circuit in the nanometer scale with dimensions that can fill the gap between electronics and photonics and carry all the electrical and optical signals, as a result, there is an improvement in the efficiency and a reduction in power dissipation for the chip, Plasmonic or SPP is the solution to this problem. Thus, plasmonic can be a bridge between photonics (broadband) and electronics (miniature nanometer size) for communications as shown in Figure 2.5. Plasmonic has a high data transmission capacity that exceeds the data rate provided by optics. It operates at

frequencies in the light and near-infrared regions, making it higher power than that offered by optics. Furthermore, plasmonic can reduce the size of the device provided by electronics, making it compatible with current manufacturing techniques such as silicon on insulator (SOI) and semiconductors made of metallic oxides (CMOS). Hence, plasmonic is capable of providing many sub-wavelength optical components combined together in the same structure to prepare for the future optical computer industry (optical integrated circuits).

2.4 Advantages and Disadvantages of Plasmonic [51]

The advantages and disadvantages of plasmonic technology are explained in the following two subsections.

2.4.1 Advantages of Plasmonics

1- Improving the field level by several levels

2- Limiting the field to a number of nanometers

3- It is considered as a Nano photonic device (reducing the size of device)

4- It is adjustable (can be set)

5- Active coupling

2.4.2 Disadvantages of Plasmonics

1- Short-range diffusion (the highest diffusion length is a few millimeters)

2- loss

3- Nanofabrication techniques are determined by the dimensions of the structure (some structures are impractical).

4- Complicated simulation

5- More expensive than optical devices

2.5 The Theory and Working Principle of Plasmonics

Plasmonics technology constitutes a major subject of study in nano-photonics. It has been used to study optical phenomena resulting from the interaction between electromagnetic fields and free electrons in metals [52]. There are two advantages of photon-electron interactions at metal-insulator interfaces, these are the sub-wavelength diffraction, and field confinement and field enhancement. This requires nanostructures with plasmon resonance at different bands in the electromagnetic spectrum. Moreover, in order to achieve high levels of domain enhancement it must have a high quality factor (Q-factor) of metals to obtain surface wave Plasmonics. The presence of surface Plasmonics is strongly dependent on the dielectric (permittivity) constants of the metal εm and requires a negative real part of the complex dielectric constant, Re (εm) < 0 as well as Im (εm) < < - Re (εm), when the Q-factors are high, that is, small damping requires small imaginary parts of εm, hence, gold, silver, and copper meet these requirements. Because silver and gold are the most common materials in surface plasmon as confirmed by optics and spectroscopy [53]. In some cases, electromagnetic waves cannot travel through a metal when their frequencies are greater than the plasmon frequency. Plasmons that are confined at the metal-insulator interface are called surface plasmons (SP). When light is coupled to these SP points under certain conditions, they improve excess electromagnetic fields of surface plasmonic polaration (SPPs). Its longitudinal waves propagate at the metal-dielectric interface and fade away significantly from the boundary in the surrounding materials. These waves run

parallel to the propagation direction. So they cannot be excited by transverse waves. The most effective method of plasmon excitation is the use of electrons; when light excites electrons [54].

2.6 The Properties of Surface Plasmon Polaritons (SPPs) [55]

1- The SPPs waves are electromagnetic (EM) waves whose frequencies are close to the frequency of infrared or visible frequencies which can propagate along an insulating-metal or metal-dielectric interface.

2- The SPPs waves contain the longitudinal and transverse components of the electromagnetic (EM).

3- The SPPs waves contain the component of the electric field and the component of the magnetic field, as in the case of the electromagnetic wave (EM).

4- SPPs waves propagate simultaneously on the insulating and conductive layers.

5- The electric field of SPPs is related to the conductive charges (the free electrons in the metal).

6- The electric field of SPPs is perpendicular, while the magnetic field is parallel to the metal-insulating interface of metals whose conductivity is high.

7- The behavior of plasma differs from that of conventional photonics.

8- Plasma can control electromagnetic waves in nanometers

9- The power transmitted by the SPPs is concentrated in areas that are very thin at the nanometer scale where it can overcome the scattering condition.

2.7 Plasmonic Waveguides

Optical fiber communications made a revolution in the world of data transmission. It proved successful in transmitting large data over long distances and bandwidth. However, the on-chip data transmission capacity in integrated electronic circuits was for short distances and for limited speed due to the time delay caused by the nano-metallic connection. Using light as a transmitter of data enables chips in nanocircuits to fix the problem of little data transmission in electronic circuits. The traditional dielectric waveguides (DWS) direct light into a region of high refractive index surrounded by a low-intensity beam where they are subject to the principle of total internal reflection according to (Snell's law). However, the scattering limit of light in the optical fiber waveguides has been an obstacle to miniaturizing the optical waveguides. This means that light waves cannot be compressed in a field with a dimension smaller than half their wavelength in this medium. Fortunately, Nano-plasminc was able to overcome the scattering limit of light using the previously discussed SPPs. One application based on SPPs that has received significant research attention over the past decade is plasmonic waveguides (PWs), which can convert light at the sub-wavelength scale to SPPs at the metal-dielectric or dielectric - metal interface that overcomes the scattering limit. PWs are the potential technology for the development of next-generation micro-devices that have the advantages of both large operating bandwidth and real nanoscale photonics, paving the way for the future integration of high-capacity photonics and electronic devices on a scale similar to electronics. Different waveguide structures and scales of SPPs are proposed with the aim of exploiting the unique features of the waveguides of SPPs at the nanometer scale. Despite the good features of PWs, there is one major problem faced which is the trade-off between loss and confinement. Two types of PWs have been used in most modern

applications: an insulator (dialectic)-metal-insulator PWs (IMI) or (DMD) or a metal-insulator (dialectic)-metal PWs (MIM) or (MDM) as shown in this part of the thesis with its advantages, disadvantages and a comparison between them.

2.7.1 Insulator-metal-insulator (IMI) PWs

This IMI or DMD PWs is made by placing a thin metal film of less than 50 nm width between two dielectric materials of the same or different indices of refraction. This is analogous to a combination of two dielectric/metal interfaces, where the field deteriorates significantly in the metal from one interface to another. This directs two leaked waves [56-57] according to the dispersion relationship equations (2.6) for the transverse magnetic mode (TM) in the waveguide given by [74]. IMI structures include films or metallic lines that are used to guide long-range symmetric SPPs (LRSPPs). The propagation distance is tens of microns or even millimeters [59-32]. However, decreasing the thickness or width of the metal strip leads to reduced mode localization [60], with shorter propagation length [60], respectively. On the other hand, anti-symmetric short range SPPs (SRSPPs) have higher localization but shorter propagation distance as they are more suitable for integrated circuits IMI PWs [60], the IMI PWs and their propagation length shown in Figure 2.5 and Figure 2.6, respectively. An IMI configuration was used to achieve a Mach-Zehnder interferometer, a polarization splitter, and a small-slot ring.

$$\varepsilon_m k_d + \varepsilon_d k_m \tanh\left(\frac{k_m}{2} d\right) = 0 \qquad (2.6)$$

Where $\varepsilon_d \; and \; \varepsilon_m \;\; are$ dielectric constants of the insulator and metal

and d is representing thin metal thickness.

$$k_d = [\beta^2 - \varepsilon_d k_o{}^2]^{1/2} \quad \text{[Dielectric Wave Number]} \quad (2.7)$$

$$k_m = [\beta^2 - \varepsilon_m k_o{}^2]^{1/2} \quad \text{[Metal Wave Number]} \quad (2.8)$$

$$k_{\circ} = \frac{2\pi}{\lambda_{\circ}} \quad \text{[Free Space Wave Number]} \quad (2.9)$$

β is the propagation constant represented by the effective refractive index of the waveguide (SPP). As in equation (2.10) .

$$n_{eff} = {}^{\beta}/_{k_0} \quad (2.10)$$

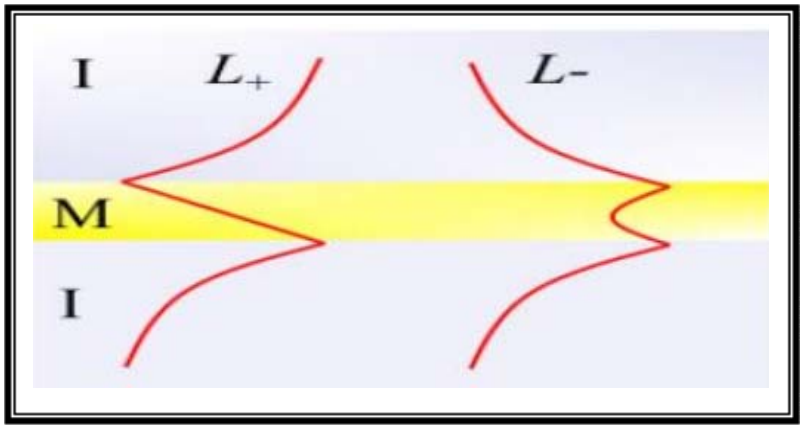


Figure 2.5 Schematic diagram of the IMI. The red lines in the two panels are the characteristic electric field profile in the two metal slab waveguides with a core thickness of z = d. The anti-symmetric mode, corresponding to the solution of L+; the symmetric mode, corresponding to the solution of L-. The wave propagates along x direction [61]

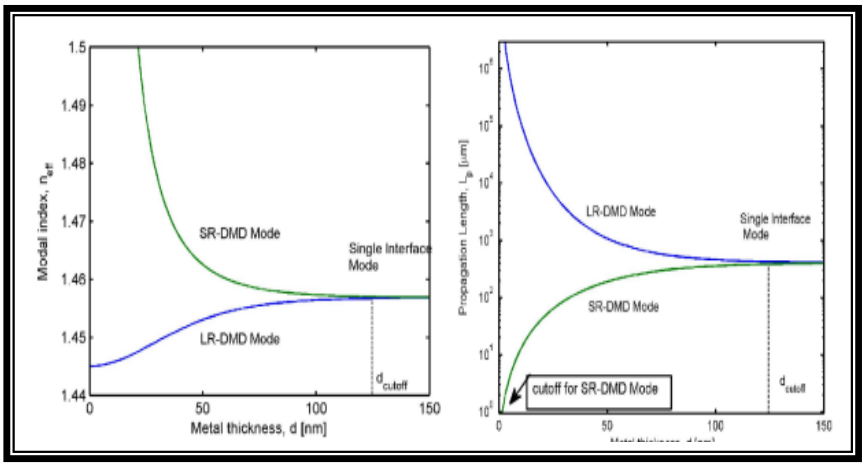


Figure 2.6 The propagation length and the modal index of the IMI waveguide mode [62]

2.7.2 Metal-insulator-metal (MIM) PWs

The second configuration that allows sub-wavelength confinement and integration is the MIM or MDM plasmonic waveguide structure as shown in Figure 2.7. As the metallic gap decreases, the propagation constant will increase, resulting in more confinement of the mode. Although this structure has short propagation lengths compared to IMI, it has a strong light-confinement mode, which can be easily used in photonic chips, and it is not affected by radiation or interference [56-58]. The dispersion relationship for the MIM structures is given by equation (2.11) [63]. Figure 2.8 shows the propagation length and modal index of the MIM waveguide. The mode corresponds to a change in the thickness of the dielectric d. At a few nanometers of the dielectric thickness, the mode coefficient of modal index of MIM is high, and it decreases with increasing insulator thickness until it reaches the dielectric thickness, where the modulus coefficient of MIM mode approaches the single interface SPP, while the propagation length increases with the thickness of the insulator.

$$\varepsilon_d k_m + \varepsilon_m k_d \tanh\left(\frac{k_d}{2} d\right) = 0 \tag{2.11}$$

where *d* is dielectric thickness.

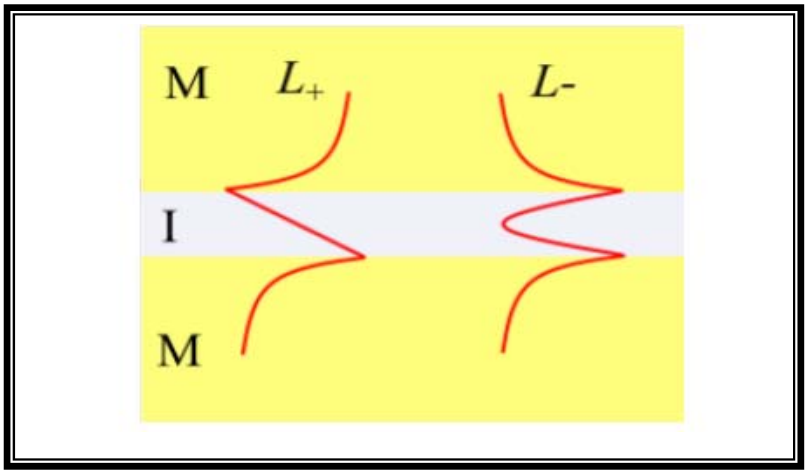


Figure 2.7 Schematic diagram of the MIM [64]

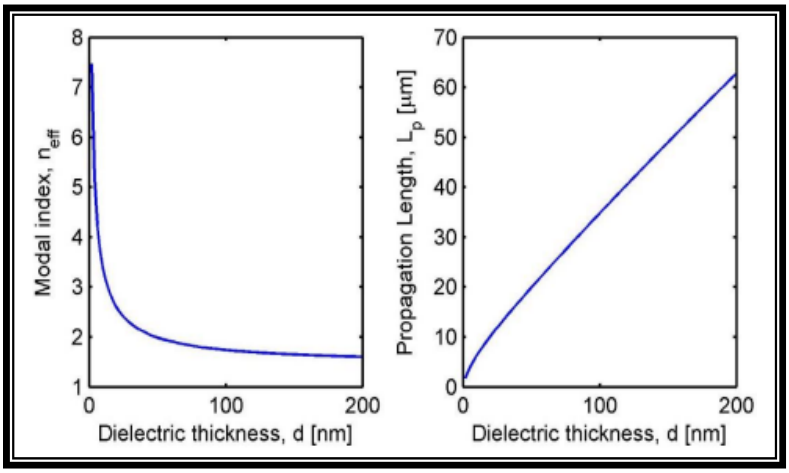


Figure 2.8 The propagation length and the modal index of the MIM waveguide mode versus the insulator thickness d [62]

2.8 The differences between IMI PWs and MIM PWs

In this section, a comparison is drawn between the above two types of IMI PWs and MIM PWs using some performance evaluation parameters as follows:

1-The IMI PWs have less propagation loss while in MIM PWs have more propagation loss [65-66].

2-The IMI PWs have more propagation length while in MIM PWs have less propagation length [67-68].

3-The IMI PWs possess less confinement for light while in MIM PWs contain more confinement for light [69-70].

4-The IMI PWs have easy in manufacturing while in MIM PWs are not easy to manufacture [67-70].

5-The IMI PWs have more quality factor while in MIM PWs have less quality factor [71-73].

6-The IMI PWs have more figure of merit while in MIM PWs have less figure of merit [72-74].

7-The dimensions of the structures that are used the IMI PWs have minimum dimensions while in MIM PWs have bigger dimensions [66].

8- The IMI PWs have low coupling loss while in MIM PWs have more coupling loss [67-75].

2.9 Applications of Plasmonics

The plasmonic technology was referred to as (the next chip-scale technology) because it is one of the most effective areas in Nano-photonics research [76]. Figure 2.9 shows the application areas of the SPP. In this study, the focus was on the applications of the plasmonic waveguide, which was used in the application of the plasmonic logic gates. The SPP plasmonic waveguides has a unique property which is focusing and dealing with light in regions of small wavelengths. This makes them useful in the future in the design of integrated circuits and nano-plasma devices. Where the SPP waveguides are used in components and devices to apply several functions such as sensors and plasmonic modulators [46]. The current study focuses on the application of plasmonic logic gates due to their importance in the synthesis of integrated optical circuits in the future.

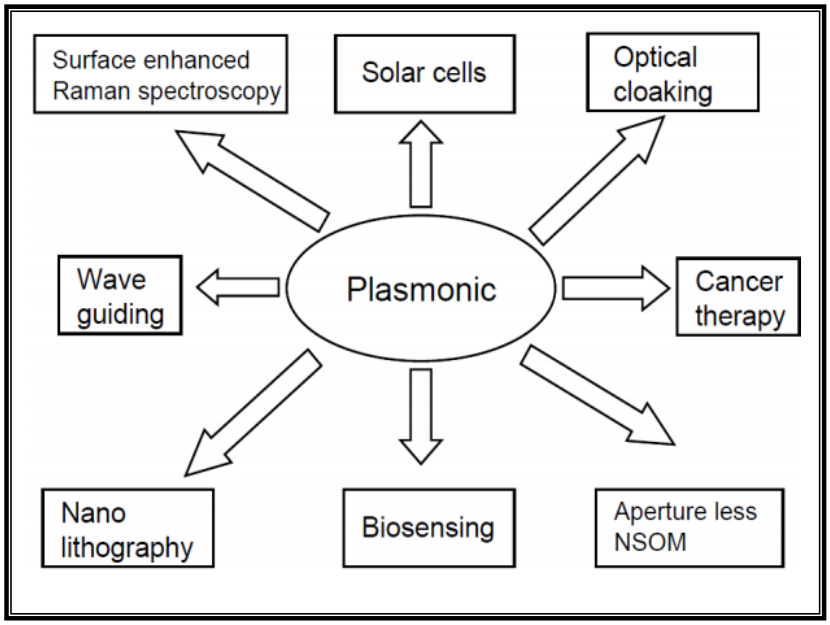


Figure 2.9 Mains areas off applications off plasmonic [77]

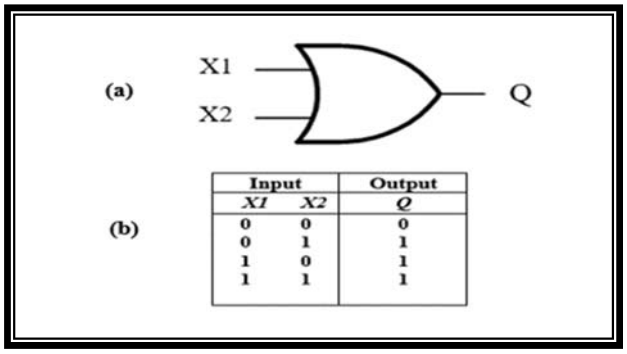
2.10 Working Principle of Conventional Logic Gate Work

In this part, the working principle of the classical logic gates (NOT, OR, AND, NOR, NAND) is explained. These gates will be carried out optically using a plasmonic waveguide.

2.10.1 OR Logic Gate

The output of OR logic gate is logic (1) if at least one of its inputs is logic (1), but if all the inputs are logic (0) its output will be logic (0). The conventional symbol and the truth table of the OR gate are shown in the Figure 2.10 (a) and (b), respectively. where the operating sign of the OR gate is (+) between the variables, and the OR operation is written in Equation as in (2.11)

$$F_{OR} = Q = X1 + X2 \tag{2.11}$$



Input		Output
X1	*X2*	*Q*
0	0	0
0	1	1
1	0	1
1	1	1

Figure 2.10 (a) Logic symbol of OR logic gate and (b) truth tables of OR logic gate

2.10.2 AND Logic Gate

The AND logic gate and its output is logic (1) if all its inputs are logic (1) otherwise its output will be logic (0). The traditional symbol and the truth table of AND gate shown in Figure 2.11 (a) and (b) respectively. The operator sign of AND gate is

represented by a point between the variables or it may be implicit without a point, then the AND operation is written by the Equation (2.12).

$$F_{AND} = Q = X1 \cdot X2 \tag{2.12}$$

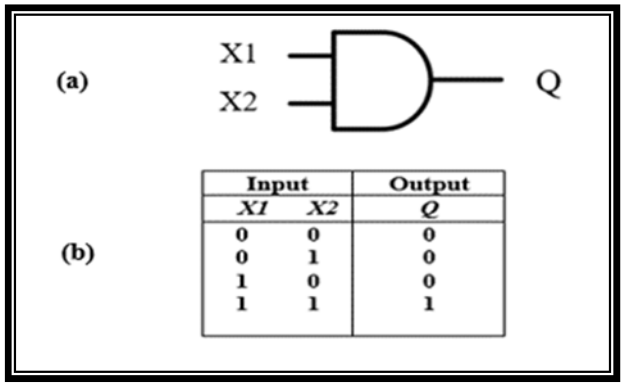
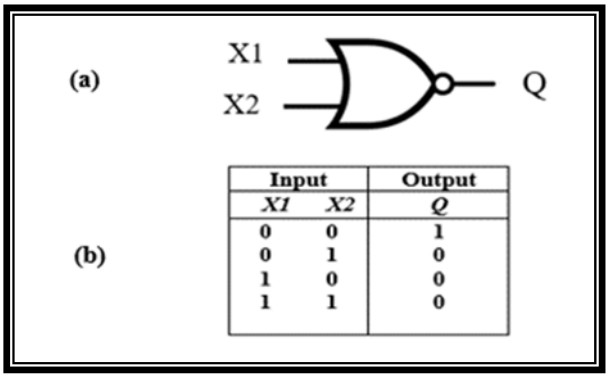


Figure 2.11 (a) Logic symbol of AND logic gate and (b) truth tables of AND logic gate

2.10.3 NOR Logic Gate

The outputs of NOR logic gate is logic (1) if all its inputs are logic (0), otherwise its output will be logic (0). The traditional symbol and the truth table of the NOR gate are shown in Figure 2.12 (a) and (b) respectively. where the operating sign of the NOR gate is (+) between the variables and the complement symbol is above it. The NOR operation is written as in the following Equation (2.13)

$$F_{NOR} = Q = \overline{X1 + X} \tag{2.13}$$



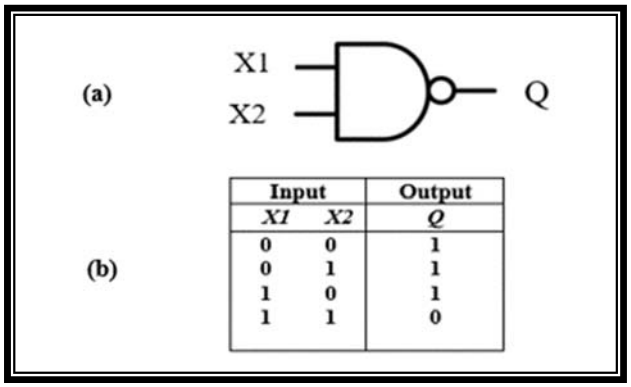
Input		Output
X1	*X2*	*Q*
0	0	1
0	1	0
1	0	0
1	1	0

Figure 2.12 (a) Logic symbol of NOR logic gate and (b) truth tables of NOR logic gate

2.10.4 NAND Logic Gate

The output of a NAND gate is logic (0) if all its inputs are logic (1), otherwise its output will be logic (1). The traditional symbol and truth table of NAND gate is shown in Figure 2.13 (a) and (b) respectively. where the NAND operation sign is point between the variables and the complement symbol is above. The NAND operation is written as an Equation as in (2.14).

$$F_{NAND} = Q = \overline{X1 \cdot X2} \tag{2.14}$$



Input		Output
X1	*X2*	*Q*
0	0	1
0	1	1
1	0	1
1	1	0

Figure 2.13 (a) Logic symbol of NAND logic gate and (b) truth tables of NAND logic gate

2.10.5 NOT Logic Gate

It is called the NOT gate or the inverter to implement the complementary concept in transposition algebra. The traditional symbol and truth table of the NOT gate are shown in Figure 2.14 (a) and (b) respectively. The output logical value of the NOT gate is simply the complement of the logical value of its input, as in Equation (2.15).

$$F_{NOT} = Q = \bar{X} \tag{2.15}$$

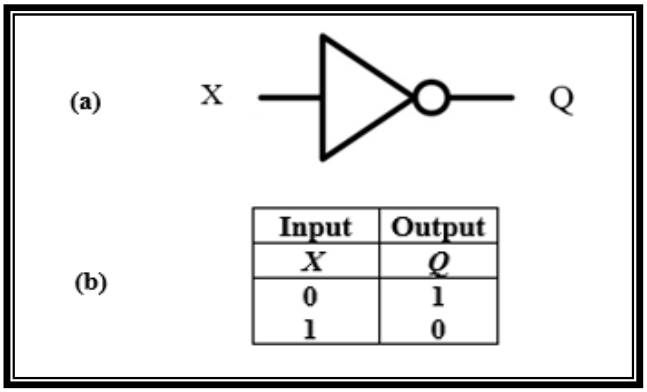


Figure 2.14 (a) Logic symbol of NOT logic gate and (b) truth tables of NOT logic gate

2.11 Literature Survey

Due to the importance of the photo-plasmonic gates and their working principle which depends on the sub-wavelength which can overcome the problems of electronic devices such as overheating and optical devices such as dispersion, photo-plasmonic gates technique has become a concern of many researchers recently. This is because plasmonic logic gates have become one of the basic components in nano-photonic integrated circuits and many optical signal processing systems. Different studies have been published proposing plasmonic structures to achieve plasmonic logic gates. The following are some of these proposed studies.

In a research paper, a structure was suggested to execute a plasmonic optical logic gate type NOT. The structure was established while utilizing the plasmonic waveguide of (MIM) type. The suggested gates have been numerically investigated employing the 2D-FDTD. In principle, the suggested gate was executed via altering the state of the control port so as to inspect if the outgoing field would propagate within the waveguide or it would not. Small sized nano-ring plasmonic waveguides of the (MIM) type have been adopted in addition to the size of the suggested structure. It was as approximately sizable as (2.4 μm × 3 μm) while the maximum transmission has been 65.35% [78].

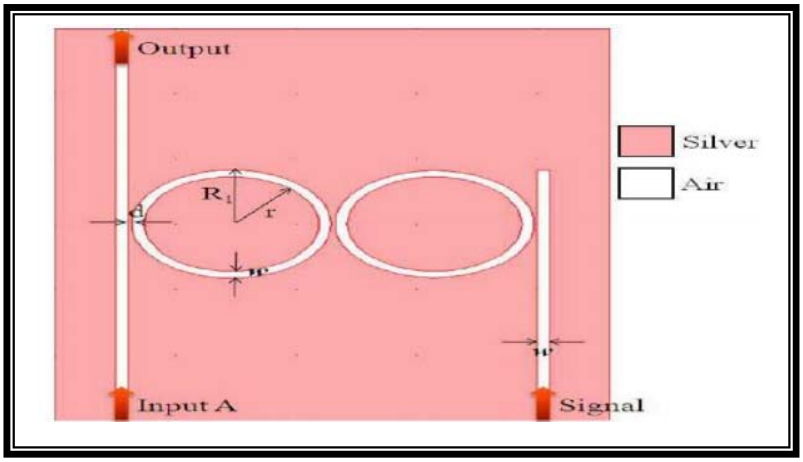


Figure 1.2 The proposed structures for [78]

In another study, XOR, XNOR which represent plasmonic optical logic gates have been suggested. These gates were established on various resonators. The resonators were Square ring resonators along with eight-sided ring resonators, and MIM resonators. All of the suggested gates have been numerically investigated employing the (2-FDTD). Practically, the performance of these gates was thoroughly calculated by means of the contrast ratio. The gates XOR and XNOR have been reported to reach the value of 22.66 - 22.9 dB in the case that the resonator adopted was of the square

type. Correspondingly, the contrast ratios reached the value of 23.01 - 23.53 dB at the event that the employed resonator was of eight-sided type for the suggested gates [79].

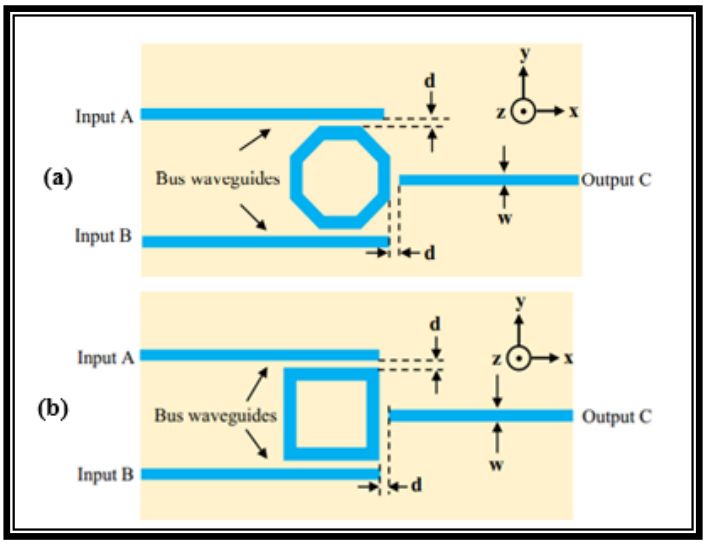


Figure 1.3 (a) The proposed structures Using octagonal resonator for implementation XOR and XNOR plasmonic logic gates (b) The proposed structures Using square resonator for implementation XOR and XNOR plasmonic logic gates for [79]

Few researchers suggested plasmonic logic gates (AND, NOT, NOR) to be executed within 2 structures. The gates have been established in accordance with the structures of plasmonic waveguides of the (MIM) type. A square ring resonator has also been utilized in the suggested structure. The size of the first structure measured 750 nm x 900 nm for the purpose of executing the NOT gate. However, the size of the 2nd suggested structure measured 1.5 µm x 1.8 µm for the two gates: AND and NOR. It is worth noting that the maximum transmission for the two structures reached 70% and 90%. Finally, the wavelength that has been exerted on these gates reached the value of 1535 nm [80].

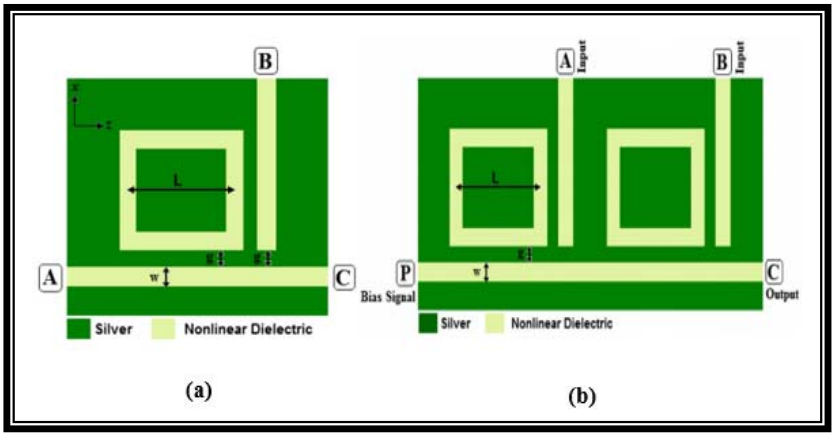


Figure 1.4 (a) The proposed structure for implementation NOT plasmonic logic gates (b) The proposed structure for implementation AND and NOR plasmonic logic gates for [80]

In a different study, two structures have been suggested to execute four optical plasmonic logic gates. They include (NOT-NAND-XOR-XNOR). The structure has been founded on a disc resonator and a plasmonic waveguide. The dimensions of the suggested structures have been as follows: 1220 × 1120 nm. The maximum contrast ratio reached 26 dB. Nonetheless, the exerted wavelength equals 525 nm. It is worth mentioning that all the gates have been investigated adopting the 2-FDTD method. The ideal performance has been achieved by the XOR gate whereas the transmission of this gate that have been attained equaled 42% [81]

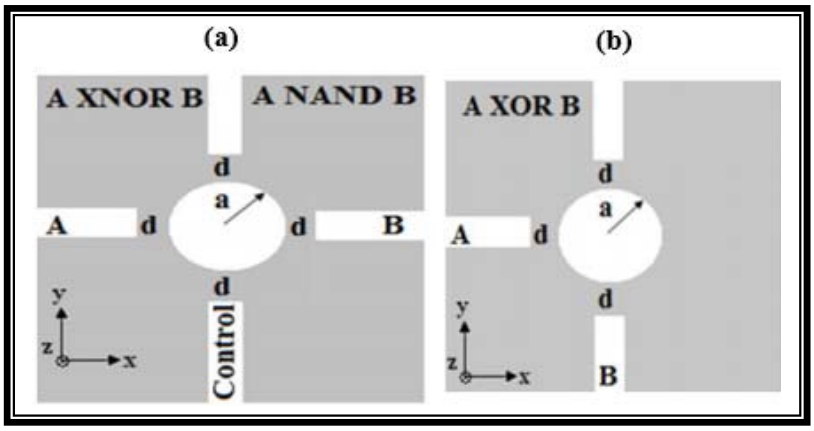


Figure 1.5 (a)The proposed structure for implementation NAND and XNOR plasmonic logic gates (b) The proposed structure for implementation XOR plasmonic logic gates for [81]

Another study suggested the execution of logic gates: AND, OR, NOT, EX-OR. They have been established by employing a matrix waveguide. The structure comprised only 1 input port as well as 3 output ports. It is crucial to indicate that the waveguide length (L) have been altered to execute these gates. Also, note that if L1 equals 0.68 μm, it should correspond to for the OR and NOT gate. However, if L2 equals 0.38 μm, it corresponds to the AND gate. And if L3 equals 0.32 μm, then it corresponds to the XOR gate. Conversely, the maximum contrast ratio calculated has been dB 13.98. A suitable waveguide length has been adopted to execute the functions of the suggested gates via indicating both of the input as well as the output ports along with the suitable value for threshold of transmission in which the waveguide lengths of the suggested gates are dissimilar [82].

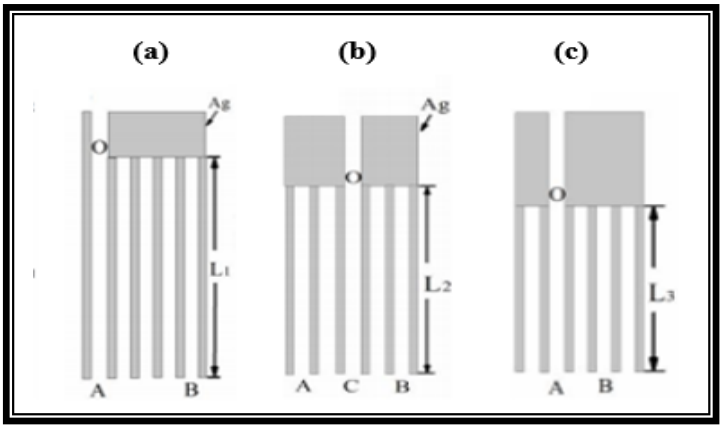


Figure 1.6 (a) The proposed structures when L1 = 0.68 µm for implementation OR and NOT plasmonic logic gates (b) The proposed structures when L2 = 0.38 µm for implementation AND plasmonic logic gates (c) The proposed structures when L3 = 0.32 µm for implementation XOR plasmonic logic gates for [82]

The authors of have suggested a structure for the purpose of executing two optical plasmonic logic gates. They are AND along with NOR. The structure relied on utilizing a ring resonator of the MIM type in addition to a plasmonic waveguide. The dimensions of the suggested structure measure $2\mu m \times 3\mu m$. According the parameters on which this structure is established, the maximum transmission has reached 84.06% at the AND gate [83].

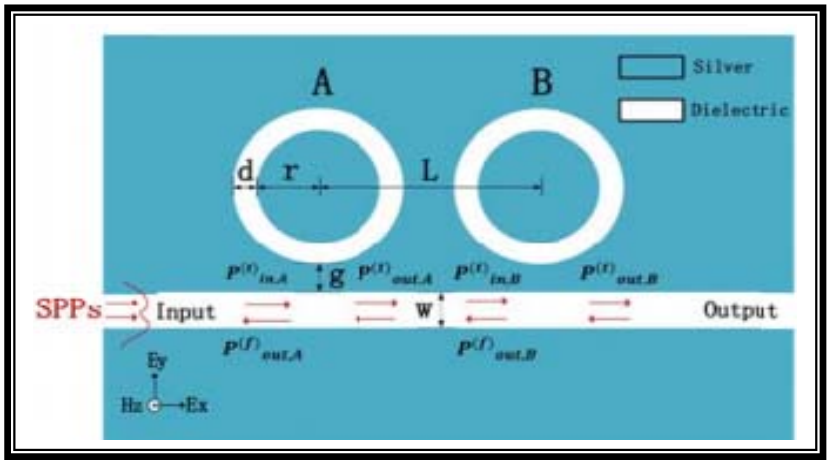


Figure 1.7 The proposed structures for [83]

In a different study, the (XOR, OR and NOT) optical plasmonic logic gates have been suggested. The structure that comprised these gates relied on the basics of the graphene-nanoribbon resonators which are found in particularly constructed structures attributed to the nano-waveguides. Such nano-waveguides functions as the logic input ports as well as the logic output ports. The results have been substantiated numerically utilizing the 2-FDTD method. The maximum contrast ratio reached the value of 8 dB. It has been acquired when the logic gates at the ON and OFF states. This is due to reliable conductivity feature exhibited by chemical capacity of graphene. The features of the suggested structure can be utilized so as to control how these gates perform [84].

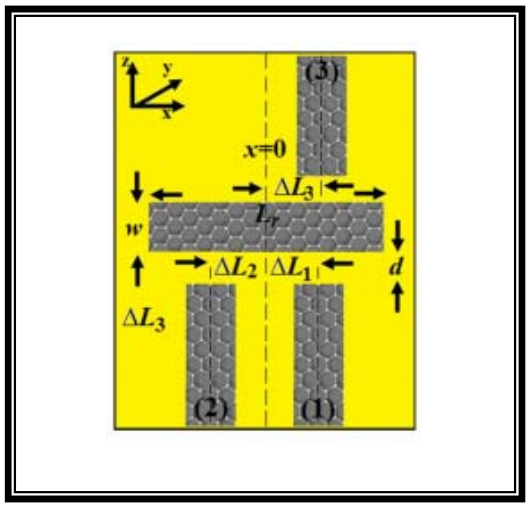


Figure 1.8 The proposed structures for [84]

Another research paper, a structure is suggested for the purpose of executing two optical plasmonic logic gates, namely OR along with NOR. This structure has been suggested relying on linear waveguides as well as vertical-linear cavities. The vertical-linear cavities exploits plasmonic structures of the MIM type which exhibits a high contrast ratio. The length of linear waveguide (l) equals 500 nm. The width of the waveguide (w) equals 50 nm. The vertical linear cavity (L) measures 1000 nm in length. Finally, the maximum contrast ratio achieved at the NOR gate has been around 12.36 dB [85].

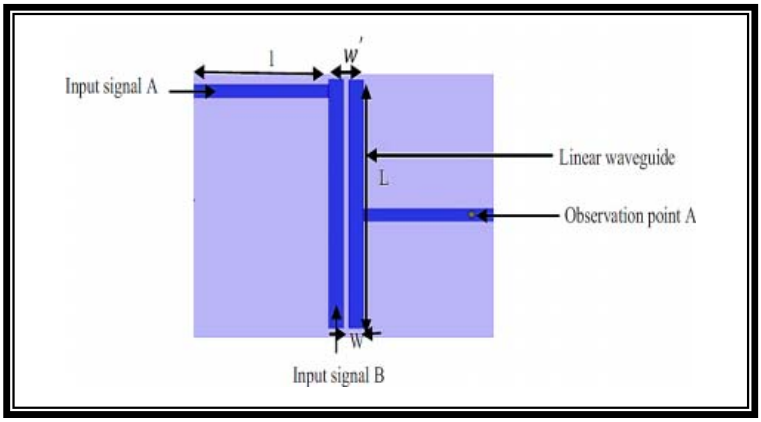


Figure 1.9 The proposed structures for [85]

2.12 Parameters of Performance Appraisal

2.12.1 Confinement

The confinement of light in the plasmonic waveguide is related to the geometry of the ephemeral fields outside the waveguide core [87]. When a ray of light passes on a flat interface placed between two different dielectrics, part of the light is reflected to the main medium and the other part is refracted in the middle of the magnetosphere. Hence, Snell's law controls the angle of reflection and refraction if $n_1 < n_2$ where ($n_1 and\ n_2$) are the refraction indexes for both materials) and the angle of incidence is greater than the critical angle θ_c as shown in Equation (2.16)

$$\theta_c = sin^{-1} \frac{n_2}{n_1} \tag{2.16}$$

The light is completely reflected back to the main medium and disperses permanently in the center of the coating, which is called total internal reflection (TIR) [88]. When the coating is a metal such as gold or silver the SPP can be available when conditions are met where energy can be transferred from the light wave excited to the free electron to form SPP that propagates on the surface of metal insulator. SPP has a wavelength

shorter than that of free light, as the shell can be made too thin, which leads to rapid energy deterioration in the metal where the sandwich structure is more complex.

As for the conventional dielectric waveguide, the sub-wavelength to confine light cannot be achieved because of the scattering that limits it. The plasmonic waveguide which is an MIM structure the resonant wavelength, the thickness of the base layer and the thickness of the film have a major role in achieving sub-wavelength confinement of light in the waveguide core. On the other hand, the confinement factor in IMI PWs waveguides is less than it is in MIM PWs waveguides as explained in the comparison between these two types above

2.12.2 propagation Length

The propagation length is defined as the distance that enables the pattern to travel before the energy density dissipates $\frac{1}{e}$ of its original value [64-89] as described by Equation (2.17)

$$L_{SPP} = \frac{1}{2im[\beta]} = \frac{1}{2k_{spp\ im}} = \lambda_0 \frac{\varepsilon_{re}^2}{2\pi\varepsilon_{im}} \{\frac{\varepsilon_{re}+\varepsilon_2}{\varepsilon_{re}\varepsilon_2}\}^{3}/_{2} \qquad (2.17)$$

where ε_{re} is the real part of the complex dielectric constant (permittivity) of the metal, ε_{im} is the imaginary part of the complex dielectric constant (permittivity) of the metal, $k_{spp\ im}$ is the imaginary part of the propagation constant and ε_2 is the permittivity of the insulating medium.

2.12.3 Quality Factor

It is the ratio between the propagation length and the resonant wavelength [88] as shown in Equation (2.18) [72]

$$Q_{SPP} = {}^{2\pi L_{SPP}}/_{\lambda_{SPP}} \tag{2.18}$$

2.12.4 Figure of Merit

The (FoM) figure of merit is a measure of the quality of surface plasmonic waveguides. It is defined as the ratio of benefit to cost, where the benefit is the sum of the light and the cost is the attenuation [90], which can be described by the Equation (2.19)

$$\mathrm{FoM}_{confinment} = {}^{\lambda_0}/_{\delta} \tag{2.19}$$

where δ is the thickness of film medium in meters.

Chapter 3

Optical Logic Gates Founded on IMI PWs Design and Simulation

3.1 Introduction

This chapter will introduce the first structure utilizing a plasmonic waveguide and a nano-square ring resonator of the IMI type. The main function of this structure is to execute five plasmonic optical logic gates. The performance of these gates is based on the both of the constructive interference as well as the destructive interference. Both types of interference occur among the signals of input and control in relation to the output. The simulation of the structure will also focus on trying out various possibilities to achieve minimum effect of propagation direction in relation to interference. In addition, two criteria will be adopted to measure the performance efficiency of the five logic gates. They are the contrast ratio and the transmission. the finite element method analysis will be adopted to simulate this structure.

3.2 Design of The First Structure and Theoretical Background

The structure comprises five optical logic gates: AND, OR, NOT, NOR, NAND as illustrated in Figure 3.1. All of these gates operate in accordance with plasmonic principles. The structure incorporates 3 linear nano-waveguides in addition to two square ring resonators of the IMI type. Dimensions of the structure are 300 nm by 350 nm. Width of both of the center and side waveguides (Ls) are 350 nm and 215 nm respectively. The height of the linear waveguide (h) is of 15 nm. The inner rib length of the resonator (a) is 40 nm, while the outer rib length (b) is 80. The distance between the square rings and the linear waveguides (d) is 7 nm. It is worth noting that the

distance between the nano-square rings and the linear waveguides is known as the coupling distance. As for the materials out of which the structure would be made are silver and insulator which has refractive index (n) of 1.424. In this design, Johnson's and Christie's definition of silver permittivity was adopted. Note that the resonance wavelengths in the plasmonic technology are determined by the dimensions of the structure as well as the materials used in the structure. The value of the resonance wavelength is expressed in Equation (3.1) [80].

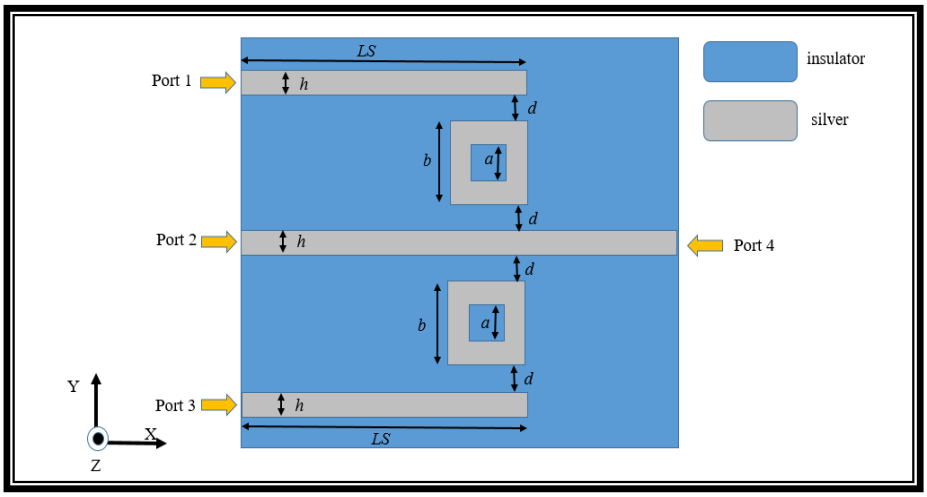


Figure 3.1 Structure for executing five optical plasmonic logic gates utilizing (IMI) PWs

$$\lambda_{spp} = 4n_{eff}b \tag{3.1}$$

Where $\boldsymbol{n_{eff}}$ stands for the refractive effective index of the metal. $\boldsymbol{b}$ represents the larger side of the nano-square ring resonator. The resonance wavelength of 1550 nm was adopted in the simulation of the structure. It is important to note that the dispersion of the transverse magnetic waveguides can be expressed as in Equation (2.6).

This structure contains 4 ports: 2 ports are designated for input; one port is designated as control port; the remaining port is designated as output port. In order to obtain the

desired output, the input and the control ports have to be activated. To measure how well each optical plasmonic gate performs, two foundations have to be established. The first criterion, the transmission which represents transferring the light from input and control ports to the output port. Transmission is the ratio of input optical power to the output optical power. A threshold has to be established for the purpose of determining logic 1 or logic 0. Accordingly, 25% is the threshold selected for simulating all the five optical gates investigated in this part of the study. The second criterion is the contrast ratio, that is, the ratio of least transmission at the ON status to the highest transmission at the OFF status. Note that the higher the contrast ratio is, the better gates will perform. Equations (3.2) [80] and (3.3) [91], illustrate the tenets of the two foundations explained above.

$$T = P_{out/}P_{in} \text{ (for the ON state and OFF state in the output port)} \quad (3.2)$$

where

T stands for the transmission.

P_{out} stands for the optical output power of the output port for ON and OFF. P_{in} stands for the optical input power of the input and control ports.

$$^{ON}/_{OFF}\, C.R(db) = 10\log_{10}[\frac{(P_{out}|ON)_{min}}{(P_{out}|OFF)_{max}}] \quad (3.3)$$

P_{out} |ON represents the optical power of the output port at the ON status, logic (1)

P_{out} |OFF represents the optical power of the output port at the OFF status, logic (0)

The level of transmission of the optical power is determined by several factors including: dimensions of the structure, the refractive index of the adopted materials, and ports locations, direction of propagation as well as the phase. It should be noted that the direction of propagation and the phase which belongs to the input signal.

Table 3.1 Illustration of the acceptability of the contrast ratio [92]

Contrast Ratio (dB) Ranges	Description	Performance
Negative value	Low	Poor and Inefficient
Less than or Equal 4 dB	Low	Accepted
More than 4 dB – 8 dB	Medium	Moderate
More than 8 dB – 12 dB	Medium	Good and Efficient
More than 12 dB – 16 dB	High	Very good and Efficient
More than 16 dB – 20 dB	High	Excellent and Efficient
More than 20 dB	Very High	Excellent and Very Efficient

As indicated earlier, the constructive and destructive interferences determine the performance of the plasmonic optical logical gates. Therefore, for the purpose of attaining constructive interferences, phase has to resemble the direction of the propagated signals through both of the input and control ports. On the contrary, for the purpose of attaining destructive interference, phase has to differ from the direction of the propagated signals through both of the input and control ports. In accordance, the order of interference is expressed in the Equation (3.4) [93].

$$m = \frac{4n_{eff}d\cos\theta}{\lambda_{inc}} \tag{3.4}$$

where

(m) stands for the interference order.

(n_{eff}) represents the refractive effect of the metal material.

(d) stands for the thickness of the metal material.

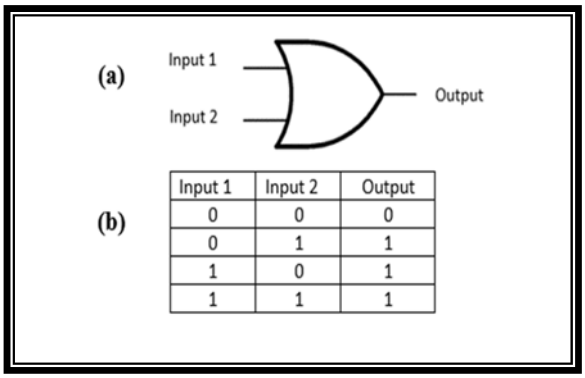
(θ) represents the phase angle of the applied or input signal.

(λ_{inc}) stands for the applied wavelength.

3.3 Results of Simulations

3.3.1 Optical Plasmonic OR Logic Gate

Drawing upon what has been presented insofar, for the purpose of executing the OR gate, the structure has to comprise ports (1) and (3) as input ports, while the ports (2 and 4) are designated as control and output ports as illustrated in Figure 3.3. The function of this gate is attained via constructive interferences found amongst the light signals propagating through the input and control ports. In this gate, there is no need to alter the phase of the input and the control ports so as to achieve the highest transmission. This is due to the fact that the output results are logic 1. At the event that the input ports are ON, constructive interference will be acquired due to the fact the direction of both of the propagation and phase are the same. As a result, the signal will double and the output will be ON too. Similarly, when one of the input ports is ON, constructive interference will also be obtained and the output will remain as ON. The last case, when both of the input ports are OFF, there will be no interference since the input signal goes through the control port resulting in weakening the transmission. See Figure 3.4 illustrates the transmission spectrum, while Figure 3.5 depicts the dispersion of the electric field on the Y-component regarding the states of the OR gate.



Input 1	Input 2	Output
0	0	0
0	1	1
1	0	1
1	1	1

Figure 3.2 (a) Symbol of the OR logic gate (b) Truth table for the OR logic gate

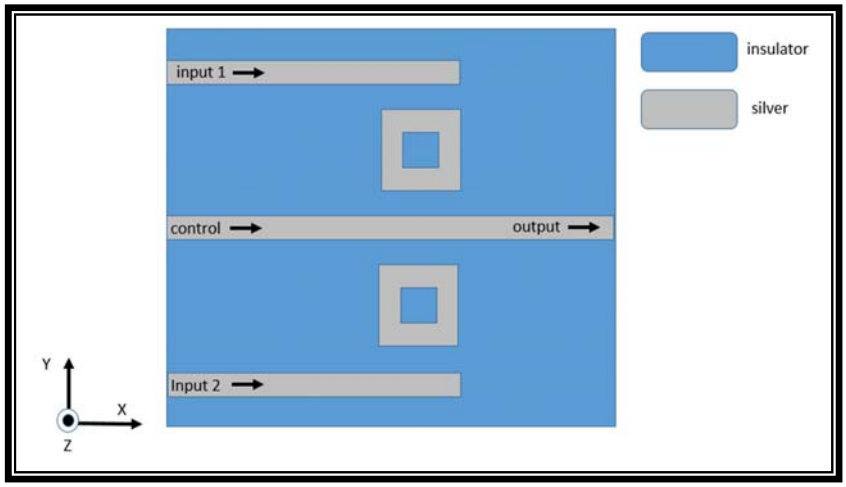


Figure 3.3 Structure for executing optical plasmonic OR logic gate

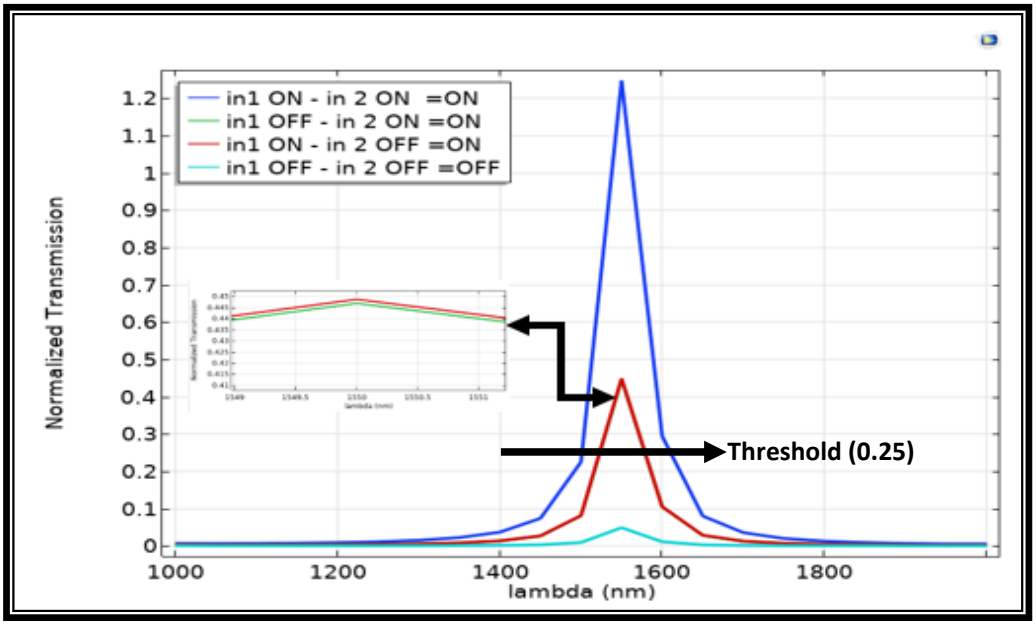


Figure 3.4 Transmission spectrum illustrating the relationship between transmission and wavelength during all states of the OR logic gate

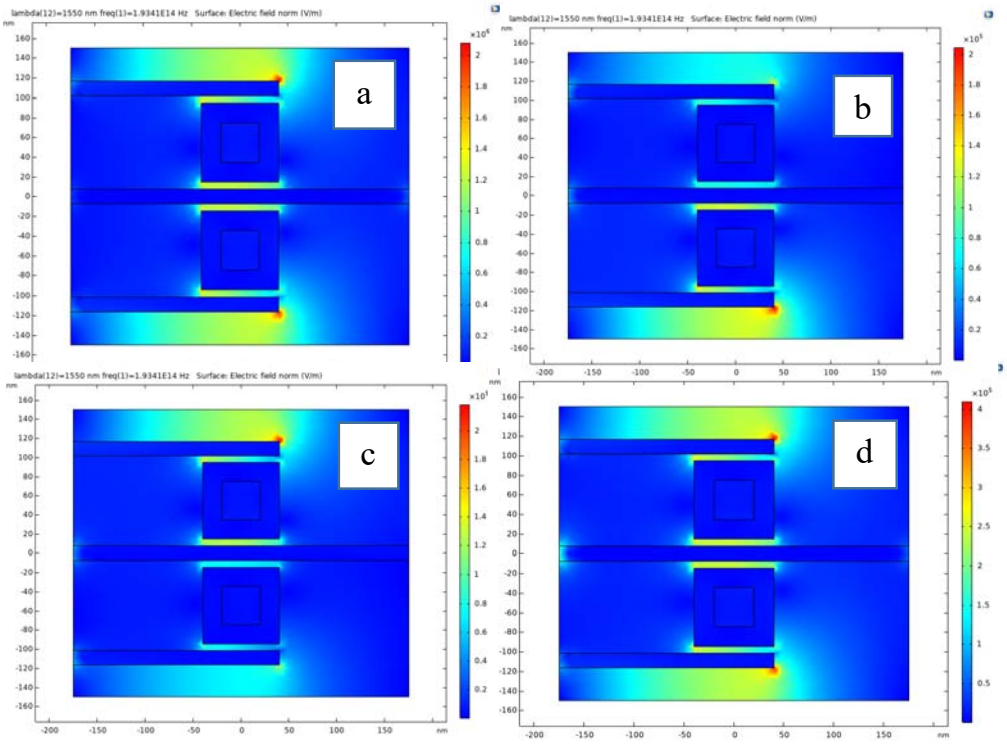


Figure 3.5 Distribution of the electric field through the Y-component (a) the input ports are OFF (b) and (c) Either the first or second input port is ON (d) the input ports are ON

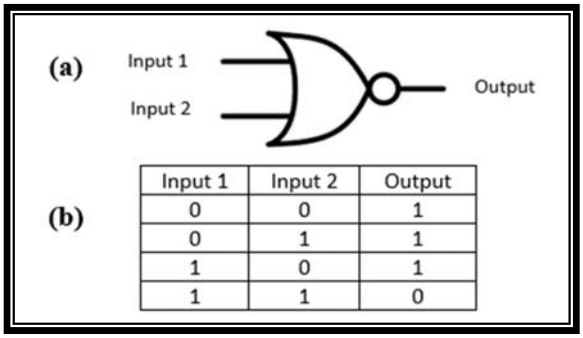
Table – 3.2 Illustration of maximum transmission (T) and calculation of the maximum contrast ratio for the optical plasmonic OR logic gate (IMI) PWs

Input optical power for single input port (P_{in}(w))	**1**	**1**	**1**	**1**
Output optical power for output port (P_{out} (w))	**1.247**	**0.446**	**0.448**	**0.048**
Input state	**on-on**	**off-on**	**of-on**	**off-off**
Output state	**On**	**on**	**on**	**off**
Minimum P_{out}|ON (W)	**0.446**			
Maximum P_{out}|OFF(W)	**0.048**			
Maximum Contrast ratio (dB)	**10.4 (dB)**			
Maximum transmission (T)	**1.247**			

3.3.2 Optical Plasmonic NOR Logic Gate

To execute the NOR gate, the input ports have to be ports two and three. However, port one has to be designated as the control port in order to reduce the strength of transmission level due to the fact that most of the cases of this gate is logic 0. Additionally, port four has to be designated as the output port as illustrated by Figure 3.7. Also, truth table of the logic gate (NOR) as well as its symbol are illustrated by Figure 3.6 (a) and (b). To clarify how the NOR gate functions, the following should be pointed out: if there no incident wave extered on the input ports, that is the OFF state, and if the control port is turned ON, then the output in fourth port will be ON. There is another possibility in which only one of the input ports happens to be ON.

Thus, the output port (four) will be turned OFF. However, if the input ports are be ON, then the phase angle of the 1st input port three has to be 180◦ as well as the phase angle of the 2nd input port two also has to be (180◦). In accordance, phase will differ between signals of the input as well as control ports. As a result, destructive interference will occur leading to weaken the transmission. To put it differently, the output port (four) will be turned OFF. For illustrative view, see Figure 3.8 which depicts the spectrum of transmission for the NOR gate. Also, see Figure 3.9 that exhibits the spread of the electric field over the Y- component for each state of the NOR gate.



Input 1	Input 2	Output
0	0	1
0	1	1
1	0	1
1	1	0

Figure 3.6 (a) Symbol of the NOR logic gate (b) Truth table of NOR logic gate

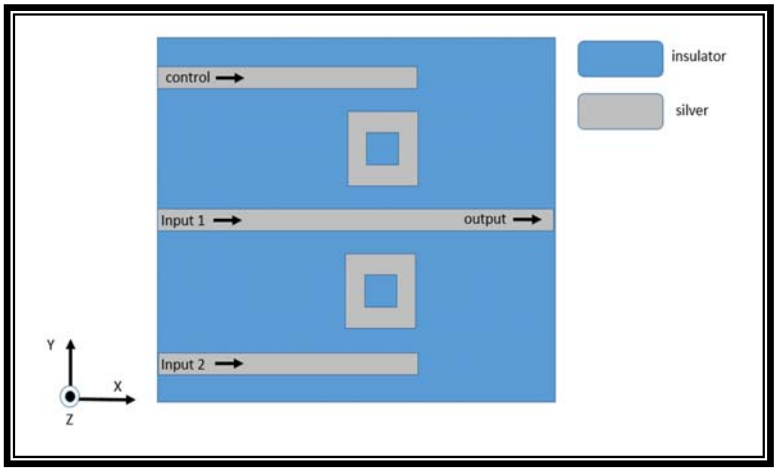


Figure 3.7 Structure of the optical plasmonic NOR logic gate

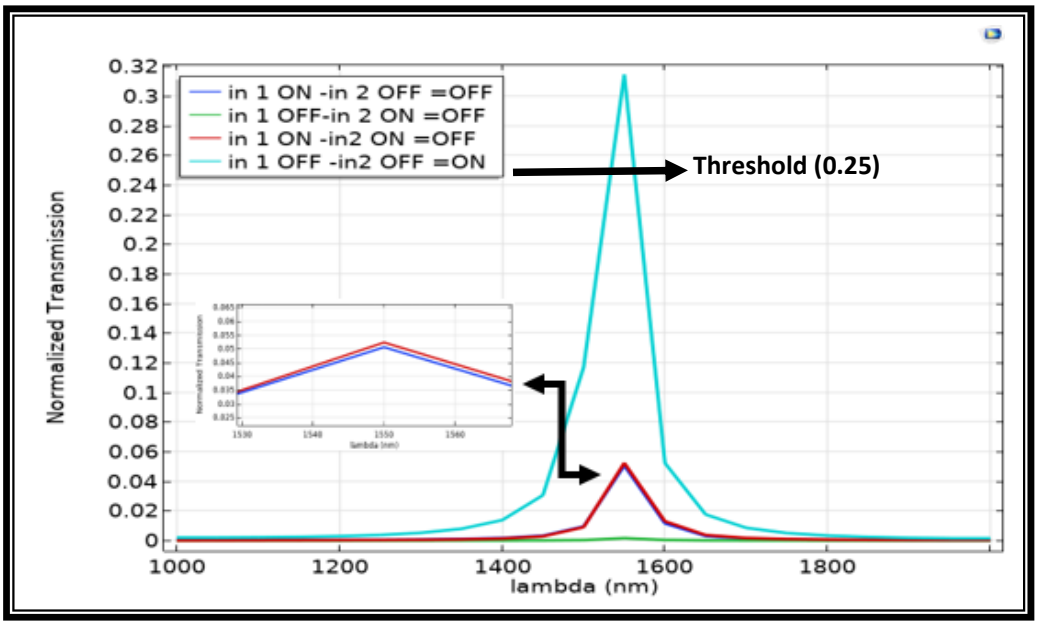


Figure 3.8 Transmission spectrum illustrating the relationship between transmission and wavelength during all states of the NOR logic gate

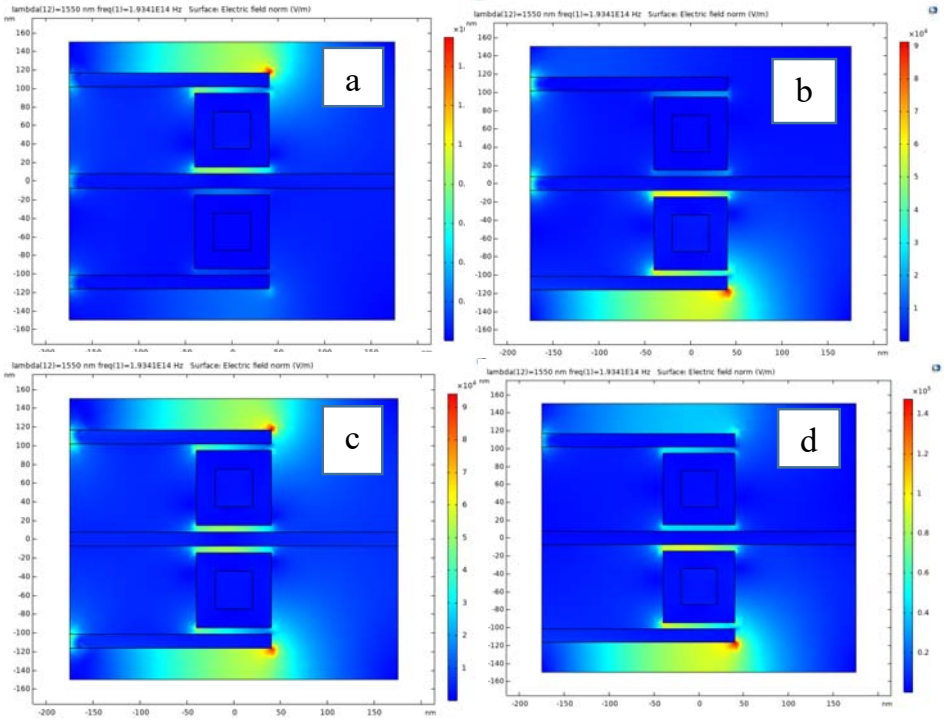


Figure 3.9 Distribution of the electric field over the Y-component. (a) inputs are ON (b) only the 1st input is ON (c) only the 2nd input is ON (d) Inputs are OFF

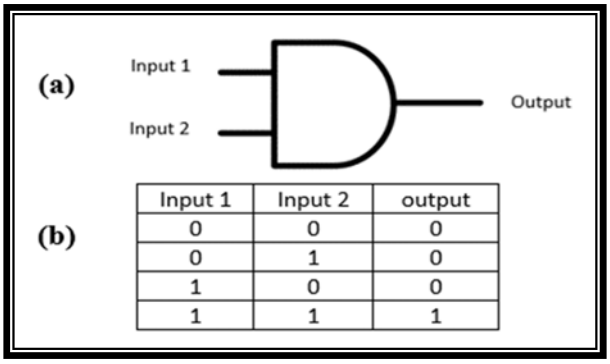
Table -3.3 Illustration the maximum transmission (T) and calculation of the maximum contrast ration for the optical plasmonic NOR logic gate (IMI) PWs

Input optical power for single input port (P_{in}(w))	**1**	**1**	**1**	**1**
Output optical power for output port (P_{out} (w))	**0.301**	**0.0506**	**0.0015**	**0.052**
Inputs state	**off-off**	**on-off**	**off-on**	**on-on**
Output state	**On**	**off**	**off**	**off**
Minimum P_{out}|ON (W)	**0.301**			
Maximum P_{out}|OFF(W)	**0.052**			
Maximum Contrast ratio (dB)	**7.6 (dB)**			
Maximum transmission (T)	**0.301**			

3.3.3 Optical Plasmonic AND Logic Gate

For the purpose of executing the AND gate of the structure, the first and third ports have to be designated as input ports while fourth port should be designated as the control port. Second port will be designated as the output port as depicted in Figure 3.11. The propagated signal of the control port should be in the opposite direction to the propagated signal that passes thorough the input ports in order to weaken the transmission. To clarify how this gate, operate, note that there are four states for this gate. The first state is when both of the input ports are ON resulting in the ON state for the output as well. The second state is when one of the inputs will be ON and the phase of the passing signal is 45◦. Note that the second state implies the third state as well

since inputs ports take turns between the OFF and ON. The output, as a result, will be logic (0) due to the difference in phase as well as in signal propagation for both of the input and control signal. The fourth state is when both of the inputs are OFF. Here, the transmission will be weak resulting in a logic (0) output. See Figure.3.10 (b) that shows the truth table of the AND gate. Also, Notice Figure.3.10 (a) which illustrates the symbol for this gate, while transmission spectrum for this gate is illustrated in Figure.3.12, and finally, Figure.3.13 depicts the spread of the electric field over the Y-component for the four states of this gate.



Input 1	Input 2	output
0	0	0
0	1	0
1	0	0
1	1	1

Figure 3.10 (a) Symbol of the AND logic gate (b) Truth table of AND logic gate

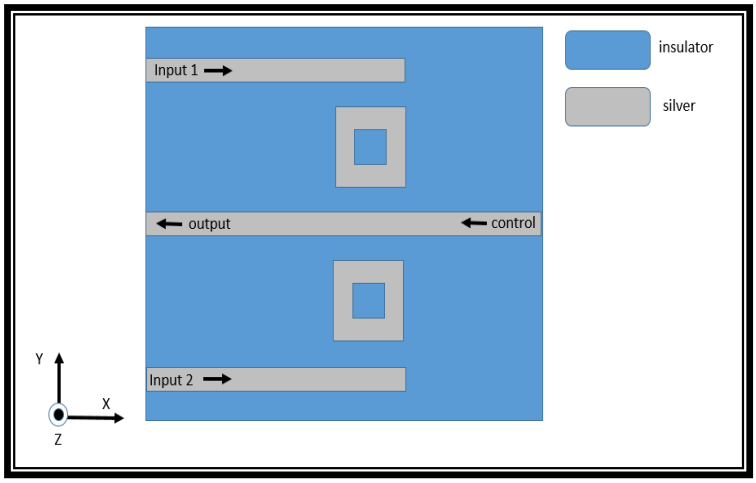


Figure 3.11 Structure for executing the optical plasmonic AND logic gate

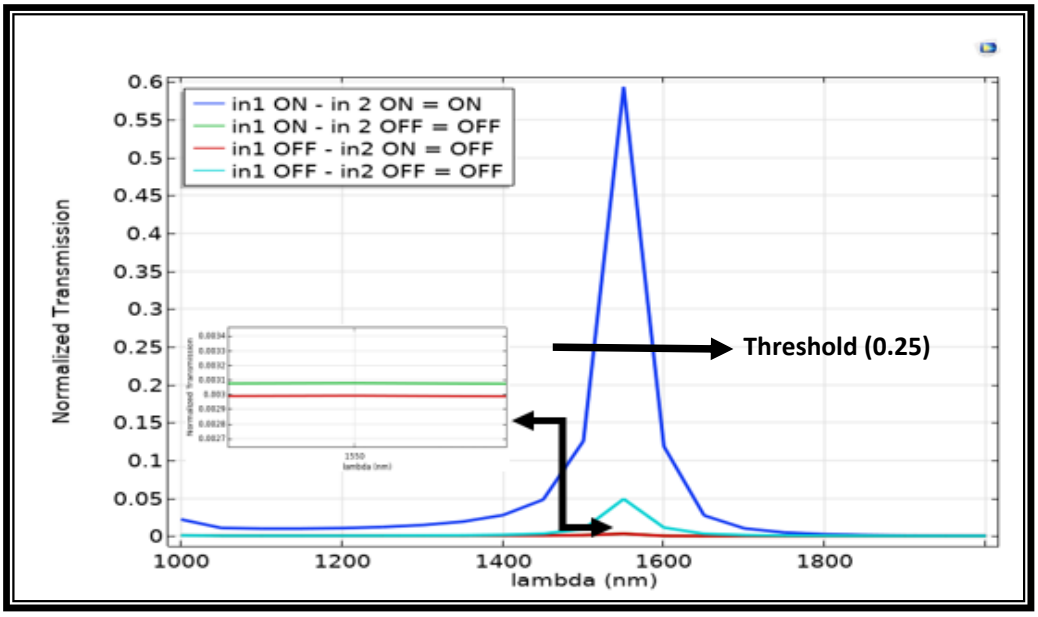


Figure 3.12 The transmission spectrum depicting the relationship between the transmission and the wavelength during all states of this gate

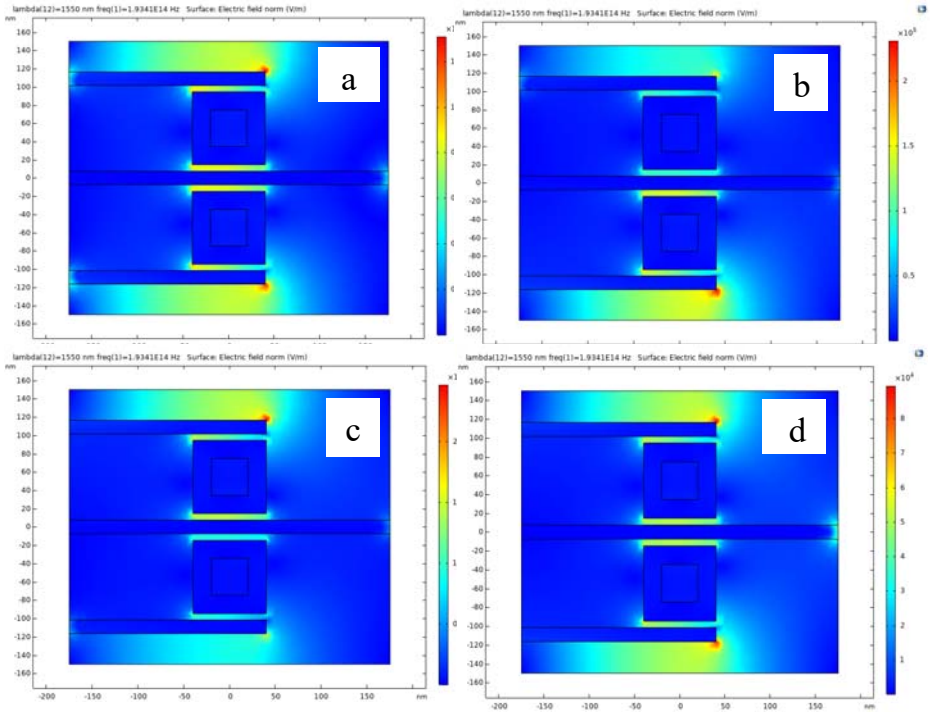


Figure 3.13 Distribution of the electric field over the Y-component. (a) the inputs are ON (b) and (c) only the 1st or 2nd input is ON (d) the inputs are OFF

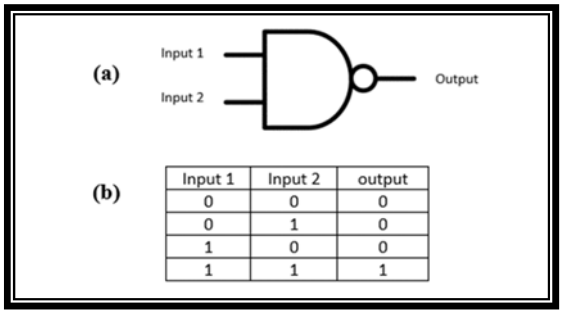
Table –3.4 Illustration the maximum transmission (T) and calculation of the maximum contrast ration for the optical plasmonic AND logic gate (IMI) PWs

Input optical power for single input port (P_{in}(w))	**1**	**1**	**1**	**1**
Output optical power for output port (P_{out} (w))	**0.59**	**0.003**	**0.0029**	**0.04**
Inputs state	**on-on**	**on-off**	**off-on**	**off-off**
Output state	**On**	**off**	**off**	**off**
Minimum P_{out}|ON (W)	**0.59**			
Maximum P_{out}|OFF(W)	**0.04**			
Maximum Contrast ratio (dB)	**11.6 (dB)**			
Maximum transmission (T)	**0.59**			

3.3.4 Optical Plasmonic NAND Logic Gate

According to the structure and for the purpose of executing the NAND gate, ports two and three should be designated as input ports whereas port one has to be the control port. Port four, then, should be designated as the output port as illustrated in Figure.3.15. To understand how this gate operates, note that both of the input ports have to be OFF while the control port has to be ON. In this state, the output port will be ON. However, in event that one of input port is ON and the control port is ON as well, then the output port will be ON too. Moreover, if both of the input ports are ON while the phase for the 1st input of the port two is 180◦ and the phase of the 2nd input of the port three is also 180◦, then there will be variation in phase between the input

ports as well as the control port resulting in destructive interferences. Accordingly, the output port will yield logic (0). For an illustrative view, notice Figure.3.16 depicting the transmission spectrum for the NAND gate. Also, see Figure.3.17 illustrating the spread of the electric field over the Y-component through the states explained above.



Input 1	Input 2	output
0	0	0
0	1	0
1	0	0
1	1	1

Figure 3.14 (a) Symbol of NAND logic gate (b) Truth table of the NAND logic gate

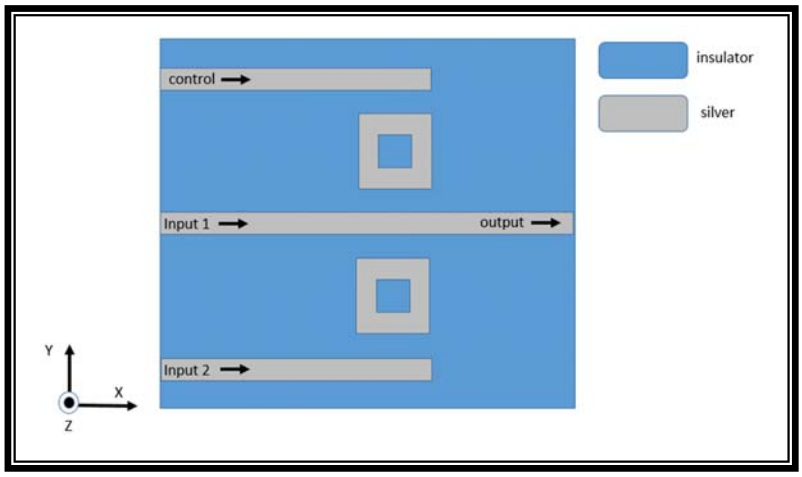


Figure 3.15 Structure for executing NAND logic gate

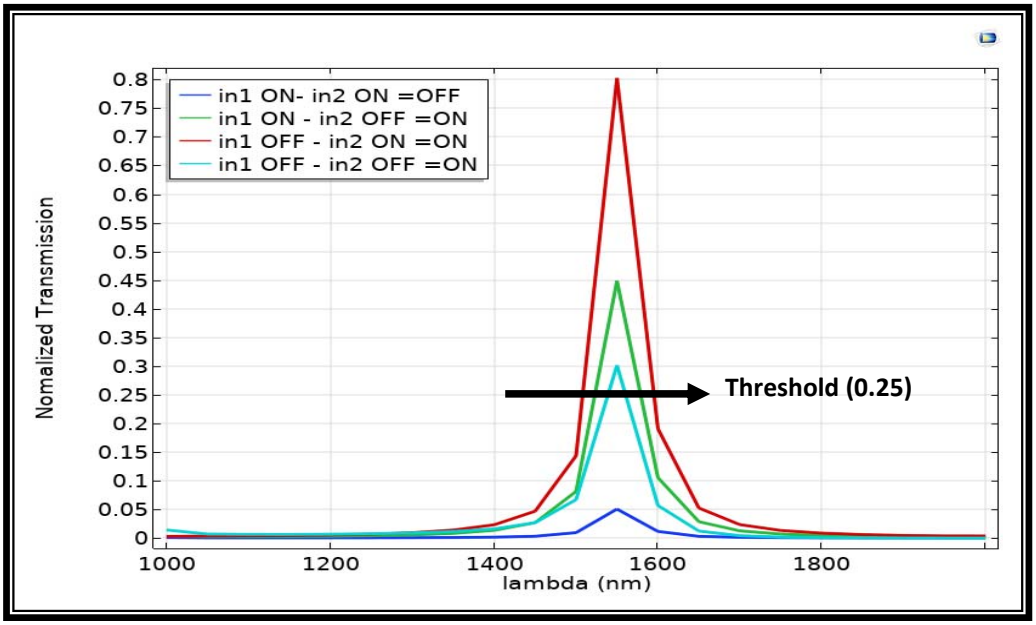


Figure 3.16 The transmission spectrum for the relationship between the transmission and the wavelength through the operating states of this gate

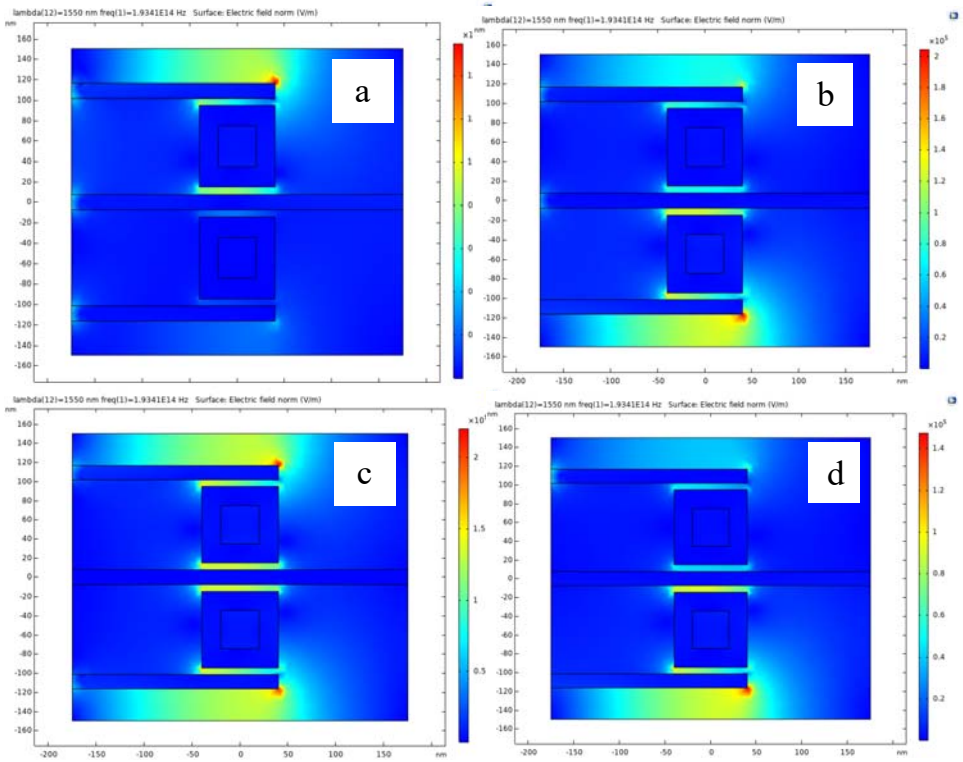


Figure 3.17 The electric field over the Y-component. (a) the inputs are ON (b) only the 1st input is ON (c) only the 2nd input is ON (d) the inputs are OFF

Table – 3.5 Illustration the maximum transmission (T) and calculation of the maximum contrast ration for the optical plasmonic NAND logic gate (IMI) PWs

Input optical power for single input port (P_{in}(w))	**1**	**1**	**1**	**1**
Output optical power for output port (P_{out} (w))	**0.448**	**0.802**	**0.301**	**0.05**
Inputs state	**on-off**	**off-on**	**off-off**	**on-on**
Output state	**on**	**on**	**on**	**off**
Minimum P_{out}|ON (W)	**0.301**			
Maximum P_{out}|OFF(W)	**0.05**			
Maximum Contrast ratio (dB)	**7.7 (dB)**			
Maximum transmission (T)	**0.802**			

3.3.5 Optical Plasmonic NOT Logic Gate

Adopting the structure, the last gate will be the Not gate to executed. It is imperative to point out that this gate has only state, either ON or OFF. Hence there will be only one input. I accordance, the arrangement of the ports will as follows: port four should designated as the input port, whereas the port one and three have to be specified as the control ports. Port two will be designated as the output port as depicted in Figure.3.19. This gate operates as the following. First, the input port happens to be ON. Similarly, the control ports are also ON. As a result, the output port will yield logic (0). Second, the input port happens to be OFF, while the control ports remain ON. The output port, thus, will yield logic (1), that is, the ON state. For more illustrative view, see

Figure.3.20 depicting the transmission spectrum for the NOT gate. Also, see Figure.3.21 illustrating the spread of the electric field over the Y-component through the states introduced above.

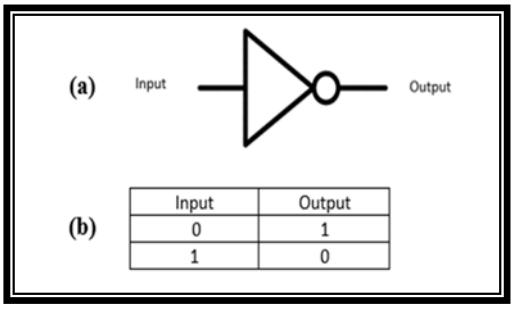


Figure 3.18 (a) Symbol of the NOT logic gate (b) Truth table of NOT logic gate

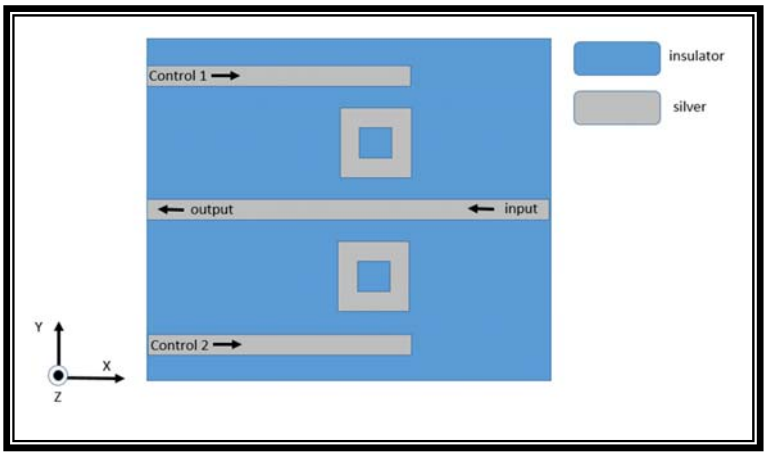


Figure 3.19 Structure for executing NOT logic gate

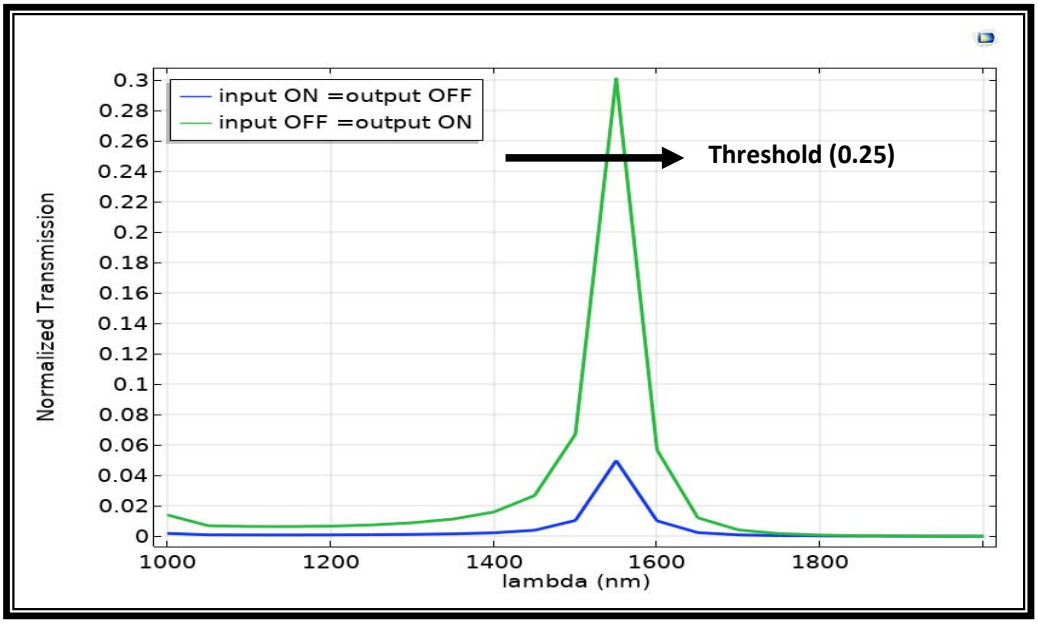


Figure 3.20 The transmission spectrum displaying the relationship between the transmission and the wavelength through the two states of this gate

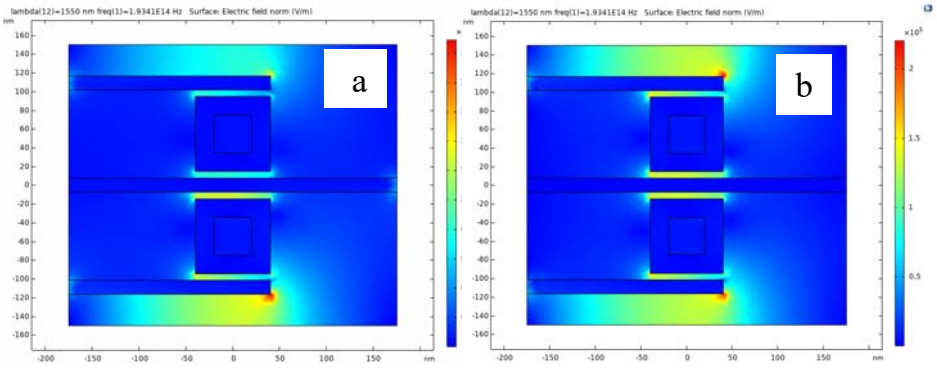


Figure 3.21 The spread of the electric field over the Y-component. (a) the input happens to be ON (b) the input happens to be OFF

Table -3.6 Illustration the maximum transmission (T) and calculation of the contrast ration for the optical plasmonic NOT logic gate (IMI) PWs

Input optical power for single input port (P_{in}(w))	**1**	**1**
Output optical power for output port (P_{out} (w))	**0.301**	**0.04**
Inputs state	**off**	**on**
Output state	**on**	**off**
Minimum P_{out}|ON (W)	**0.301**	
Maximum P_{out}|OFF(W)	**0.04**	
Maximum Contrast ratio (dB)	**8.7 (dB)**	
Maximum transmission (T)	**0.301**	

3.4 Summary

Building upon the simulation of the structure, few issues should be noted. First, the five gates were executed within a small structure in comparison to previous work. The dimensions of the structure were (300 × 350) nm. Second, the wavelength of the value 1550 nm was used for all the executed gates and one threshold of transmission was also used, which equals 25%. These gates were executed via adopting the principles of the constructive and destructive interferences amongst the signals of inputs and controls which occur through the ports of the suggested structure. It should be pointed out that the coupling distance (d) is key in determining the transmission level. The optimal coupling distance ought to be 7 nm. Notably, the contrast ratio as well as

transmission were considered the basic criteria against which the performance efficiency of the five logic gates was evaluated. In accordance, some of these gates reached higher than 100% of the transmission value. One of the gates that reached over than 100% was the OR gate scoring 124%. In a similar manner, the topmost contrast ratio reached the value of 11.6 dB as was exhibited through the performance of the AND gate.

Chapter 4

Optical logic gates Founded on MIM PWs Coupled with Slot Cavity Resonator: Design and Simulation

4.1 Introduction

In the field of optics, the tinier devices are the best; therefore, the diffraction limit of light seems like an essential limitation in the way of that field. In return, new methods have appeared to resolve this issue. One of these methods is the plasmonic technology which allows light pressure into nano-structures. this chapter suggests a all-optical logic gates based on (MIM) waveguide structure. This waveguide has an important characteristic which is restricting the applied light strongly far from the scattering limit. The structure is small compared to the applied wavelength. The optical plasmonic gates are (OR, NOR, AND, NAND and NOT). The COMSOL MULTIPHSICES (5.5) software was used for simulation by the 2-D FEM method. Hence, these five gates will be obtained by optical interference between the propagating signals through the input ports and the control ports, whose positions can be altered according to the gate needed. The implementation and simulation of the gates were all in the same structure, with the same dimensions, the same wavelength and the same transmission threshold, with applicable wavelength of (1550 nm). The performance of the plasmonic gates was tested by two criteria the optical transmission and the contrast ratio, which is the ratio between the ON and OFF states of the gate.

4.2 Design of The Second Structure and Theoretical Background

The current structure implementing (five) plasmonic optical gates, consists of a waveguide of three layers (MIM) and a rectangular nano aperture, Figure.4.1. Silver and air are used in this structure as conductive and insulating material, respectively. The waveguide dimensions is very small compared to the applied wavelength and the small size of the waveguide dimensions will give a singlet propagation pattern for TM in the waveguide (MIM), and the complex propagation constant β can be calculated by solving the dispersion relation in Equation (2.11) .

The structure in the current study has four ports, two of which are input ports, the third is a control port, and the last is an output port. The basic operations of logic gates are realized on the principle of constructive and destructive interferences between optical signals that propagate in the waveguides. the interference between the incident light signals depends on the phase of the applied light field as well as the positions of stimulating ports (input or control), in which the structure dimensions of the waveguides are as follows.

where $w = h_c$ = 100 nm is waveguide width and height the nano-slot cavity , W_c = 560 nm is the nano-slot cavity width, and g = 15 nm is the distance between the waveguide and the nano-slot cavity . The materials used in this proposed structure are silver and air. The waveguides and the nano-slot cavity are of air substance and the rest of the structure is of silver, Figure.4.1. The structure will simulate plasmonic optical logic gates (OR, NOR, AND, NAND and NOT) MIM based on PWs. All five plasmonic optical gates have the same dimensions, the same materials and the same structure. The Jonson and Christy data are used in simulations to describe the permittivity of silver, while the permittivity of air is (ε_d= 1) for the insulator, as the wavelength of resonance can be calculated by following Equation (4.1) [94] .

$$\lambda_{spp} = 2n_{eff}W_c/m \tag{4.1}$$

where n_{eff} is the refractive index of the metal, The nano-slot cavity width is w_c and m is an integer that decides the mode number which represents order of the resonance mode in the nano-slot cavity. When the mode number is equal to one, Equation (4.1) will becomes Equation (4.2).

$$\lambda_{spp} = 2n_{eff}W_c \tag{4.2}$$

According to the above equation, the structure parameters and the type of material used in the simulations are considered a rule in selecting the wavelength, for which 1550 nm was selected as it is the best option in optical communication applications. These five gates can be measured by two criteria, the first is the transmission which is the ratio between the optical power output to the optical power of the signal entering the port (input or control). The second criterion is the contrast ratio, which is the ratio between the lowest optical power in the ON state and the highest optical power in the OFF state in the output port, and the higher this ratio the better the performance of the gate, as these two criteria are described in Equations. (3.2) and (3.3) as follows.

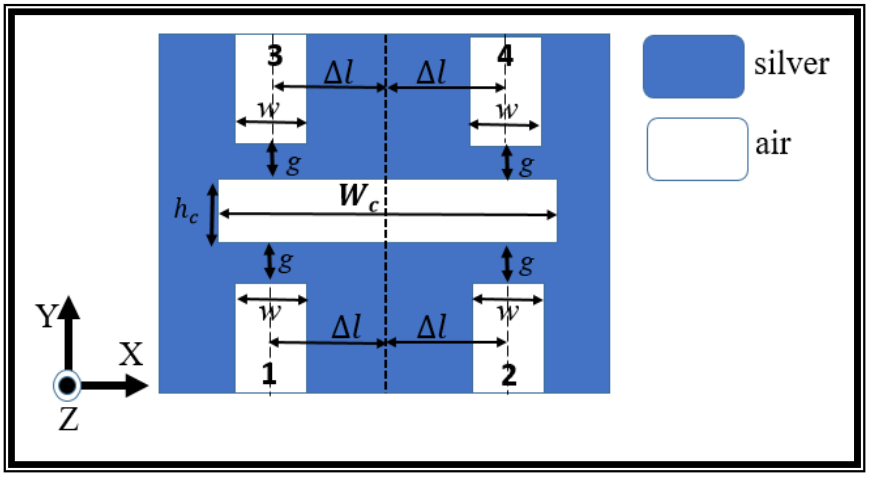
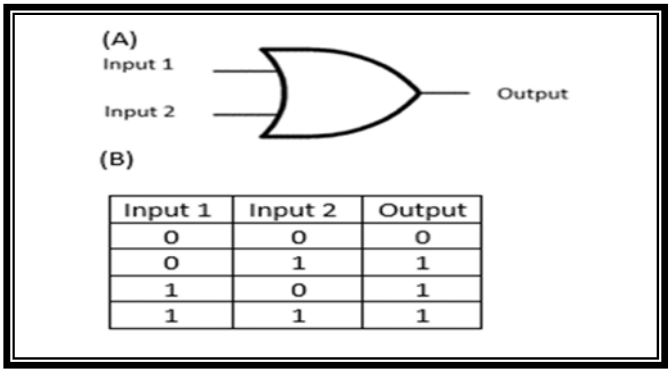


Figure 4.1 The structure to implement five optical logic gates using MIM PWs

4.3 Results of Simulations

4.3.1 Optical Plasmonic OR Logic Gate

Drawing on the discussion over the theoretical part of the structure illustrated in Figure 4.1, Δl is considered equal for all ports of all five gates. In this gate, ports (2 and 4) were considered input ports, and port (1) an output port. Port (3) is control port in this gate as shown in the structure illustrated in Figure 4.3, By examining the truth table of the OR gate and its form in Figure 4.2 (A) and (B) respectively. it can work as an OR gate and Figure 4.4 shows the transmission to the OR gate, the highest transmission obtained is 1.211% and a transmission threshold is 0.25. When one input port is ON, the output in port (1) is ON, and when the two inputs are ON, the output in port (1) is ON as well. Likewise, when the two inputs are OFF, the output in port (1) is OFF, as shown in the Figure 4.4.



Input 1	Input 2	Output
0	0	0
0	1	1
1	0	1
1	1	1

Figure 4.2 (A) OR logic gate symbol (B) OR logic gate truth table

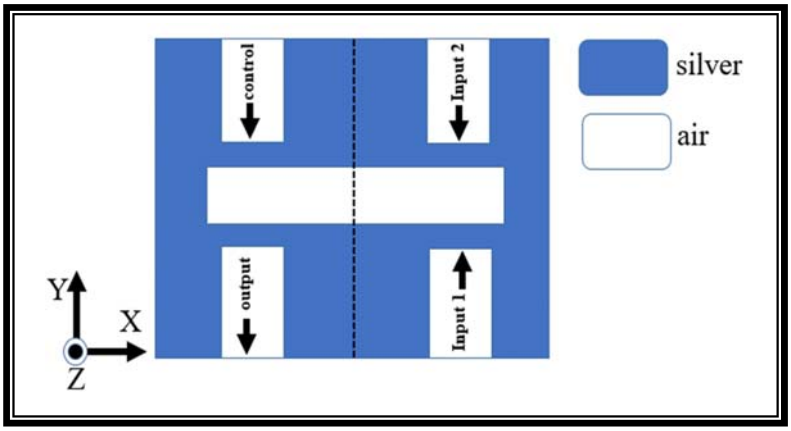


Figure 4.3 Structure for implementing an optical plasmonic OR logic gate

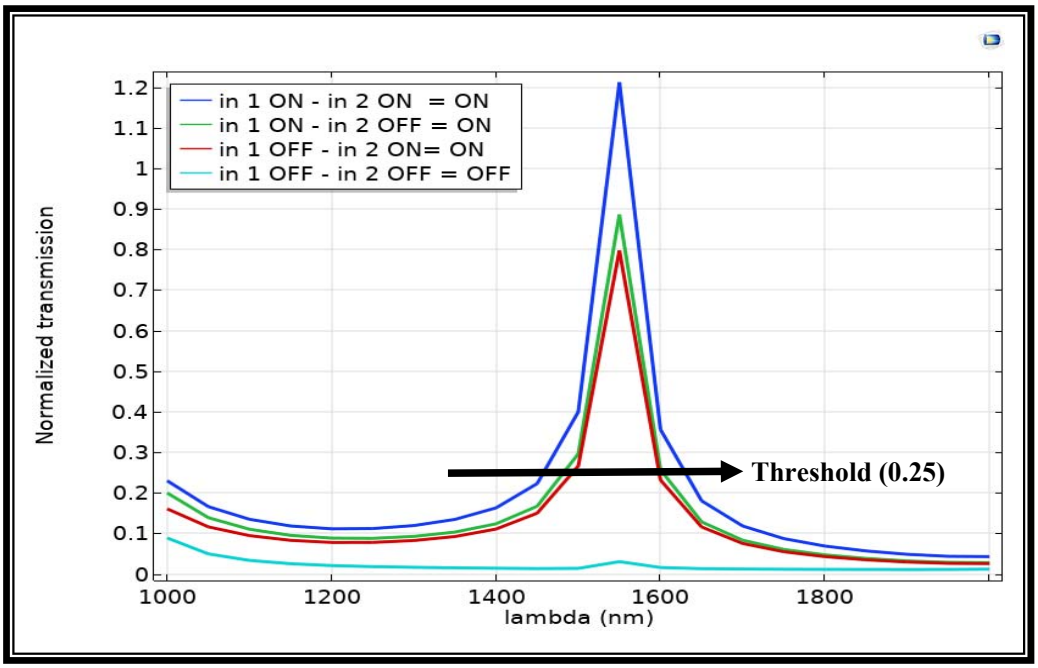


Figure 4.4 The spectrum of the transmission showing the correlation between the transmission and the wavelength for all states of the optical plasmonic OR logic gate

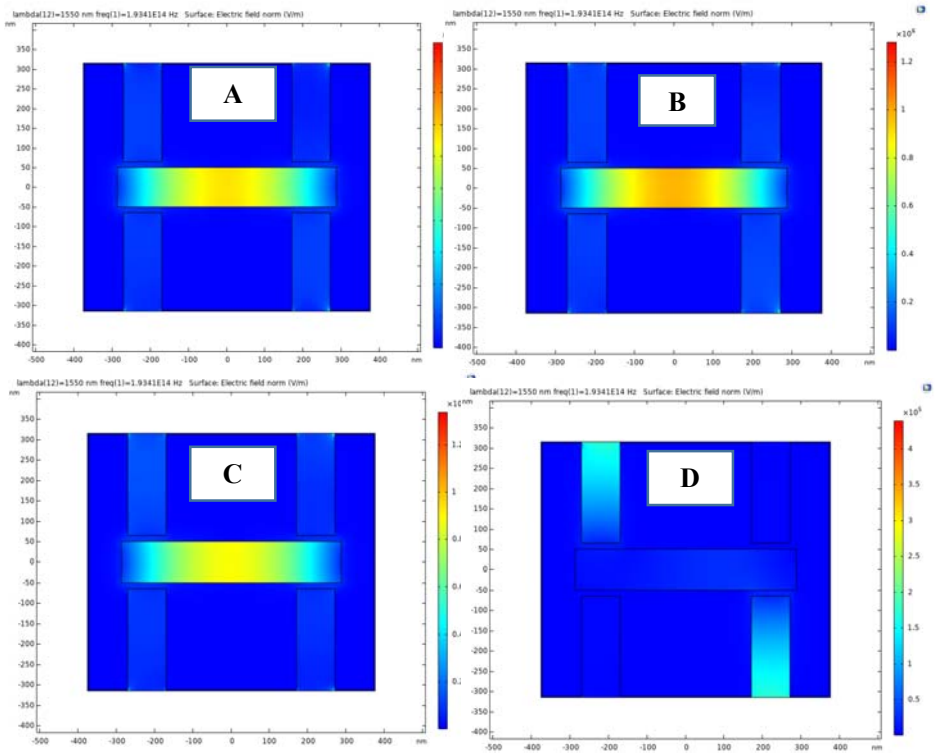


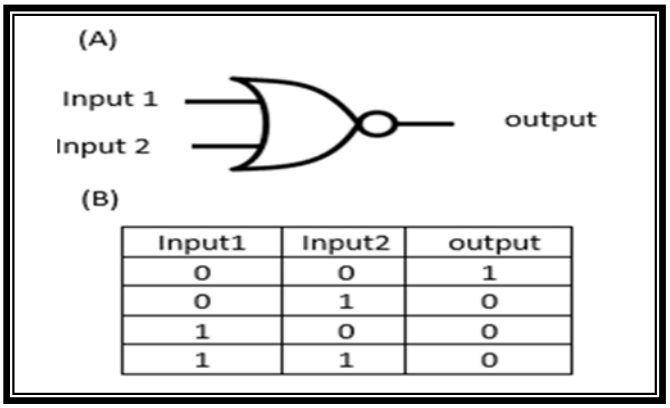
Figure 4.5 Electric field of state of OR logic gate in the structure (A) when the input in the first port is ON, (B) when the input in the second port is ON, and (C) when the two inputs are ON (D) when the two inputs are OFF

Table-4.1 Illustration the maximum transmission (T) and calculation of the maximum contrast ration for the plasmonic OR logic gate

Input optical power for single input port (P_{in}(w))	**1**	**1**	**1**	**1**
Output optical power for output port (P_{out} (w))	**1.2117**	**0.885**	**0.797**	**0.0303**
Inputs state	**on-on**	**on-off**	**off-on**	**off-off**
Output state	**on**	**on**	**on**	**off**
Minimum P_{out}|ON (W)	**0.797**			
Maximum P_{out}|OFF(W)	**0.0303**			
Maximum Contrast ratio (dB)	**14.2 (dB)**			
Maximum transmission (T)	**1.2117**			

4.3.2 Optical Plasmonic NOR Logic Gate

Drawing on the discussion over the theoretical part, ports (2 and 4) were considered as input ports, port (3) as output port, and port (1) as control port. This port is always ON as shown in Figure 4.7. As shown in the truth table of the NOR gate and its form illustrated in Figure 4.6 it can work as an NOR gate. Figure 4.8 shows the transmission of the NOR gate, as highest transmission at 0.39%. When one input port is ON, the output in port (3) is OFF, and when the two inputs are ON, the output in port (3) is OFF as well. Likewise, when the two inputs are OFF, the output in port (3) is ON, as shown in the Figure 4.8.



Input1	Input2	output
0	0	1
0	1	0
1	0	0
1	1	0

Figure 4.6 (A) NOR logic gate symbol (B) NOR logic gate truth table

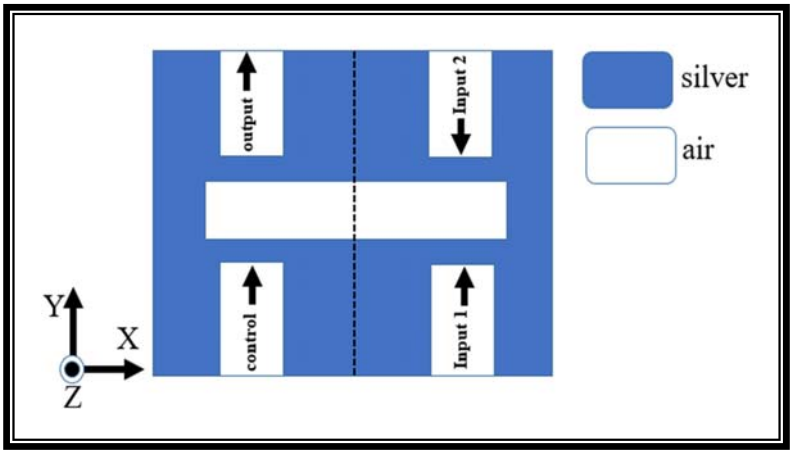


Figure 4.7 Structure for implementing an optical plasmonic NOR logic gate

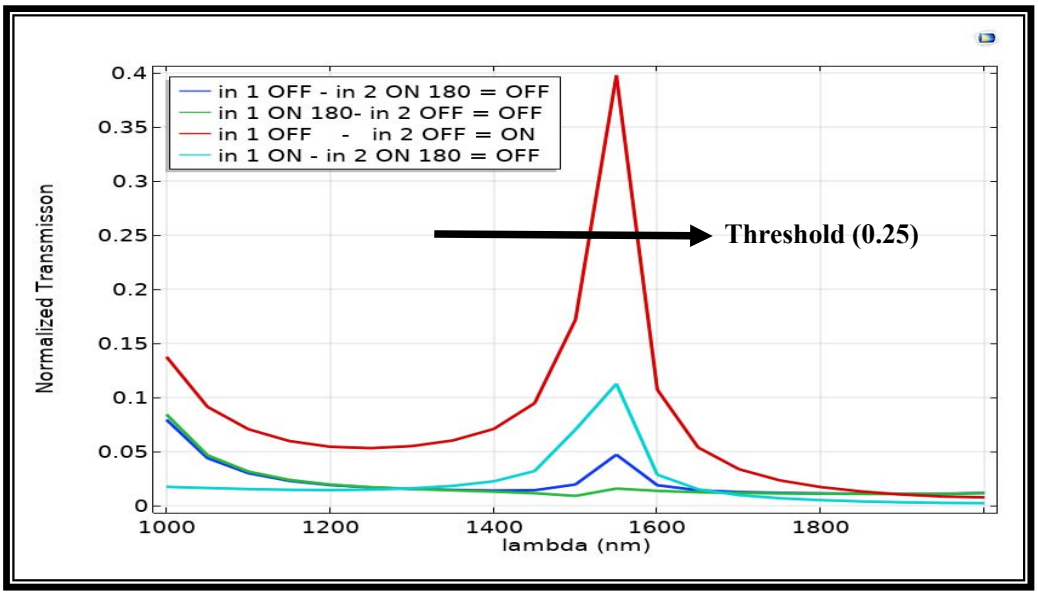


Figure 4.8 The spectrum of the transmission showing the correlation between the transmission and the wavelength for all states of the optical plasmonic NOR logic gate

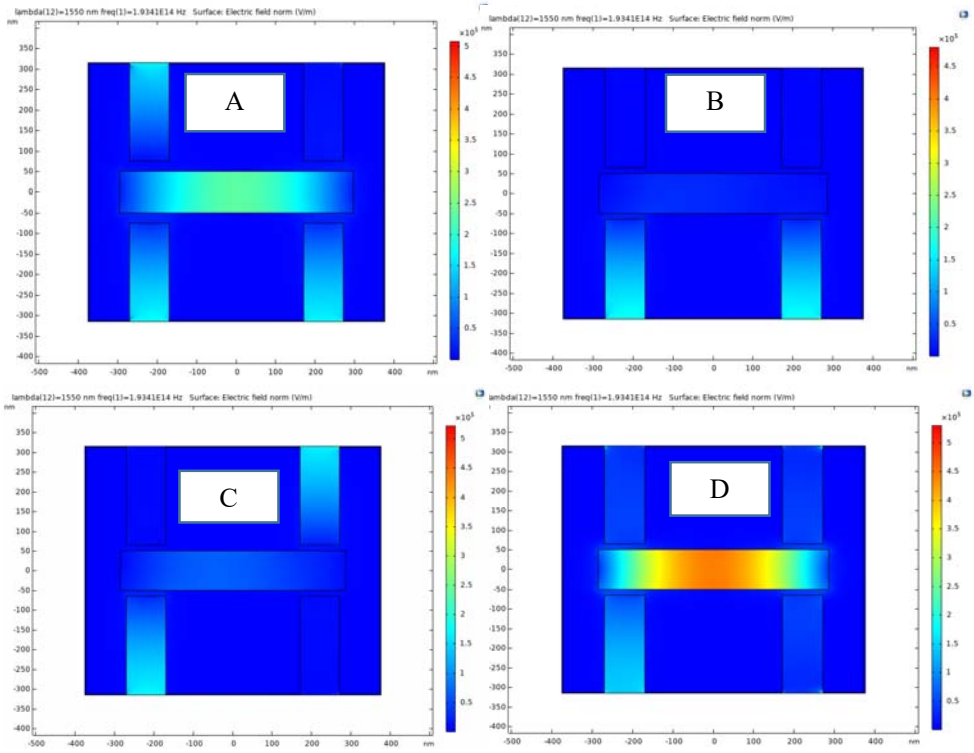


Figure 4.9 Electric field of states of NOR gate in the structure (A) when the input in the first port is ON, (B) when the input in the second port is ON, (C) when the two inputs are ON, and (D) when the two inputs are OFF

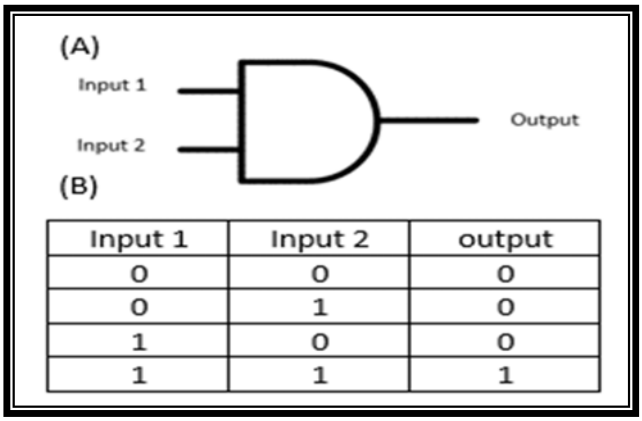
Table - 4.2 Illustrate the maximum transmission (T) and calculation of the maximum contrast ration for the plasmonic NOR logic gate

Input optical power for single input port (P_{in}(w))	**1**	**1**	**1**	**1**
Output optical power for output port (P_{out} (w))	**0.397**	**0.1125**	**0.047**	**0.015**
Inputs state	**off-off**	**on-on**	**off-on**	**on-off**
Output state	**on**	**off**	**off**	**off**
Minimum P_{out}|ON (W)	**0.397**			
Maximum P_{out}|OFF(W)	**0.1125**			
Maximum Contrast ratio (dB)	**6 (dB)**			
Maximum transmission (T)	**0.397**			

4.3.3 Optical Plasmonic AND Logic Gate

In this gate; however, the ports (2 and 3) are considered as input ports, port (4) as a control port always on ON in all cases, and port (1) as an output port as shown in Figure 4.11. As in the truth table of the AND gate and its shape in Figure 4.10, it can operate as an AND gate. Figure 4.12 shows the transmission of the AND gate, with the highest transmission obtained as 1.1%. When the first input is ON in port (2) and the phase angle of the signal applied is *0*° degrees, the output in port (1) will be OFF. On the other hand, when the second input is ON in port (3) and the phase angle of the applied signal is 0° degrees, the output in port (1) will be OFF. Likewise, when the

two inputs are ON, the output in port (1) will be ON and when the two inputs are OFF, the output in port (1) will be OFF, as shown in the Figure 4.12.



Input 1	Input 2	output
0	0	0
0	1	0
1	0	0
1	1	1

Figure 4.10 (A) AND logic gate symbol (B) AND logic gate truth table

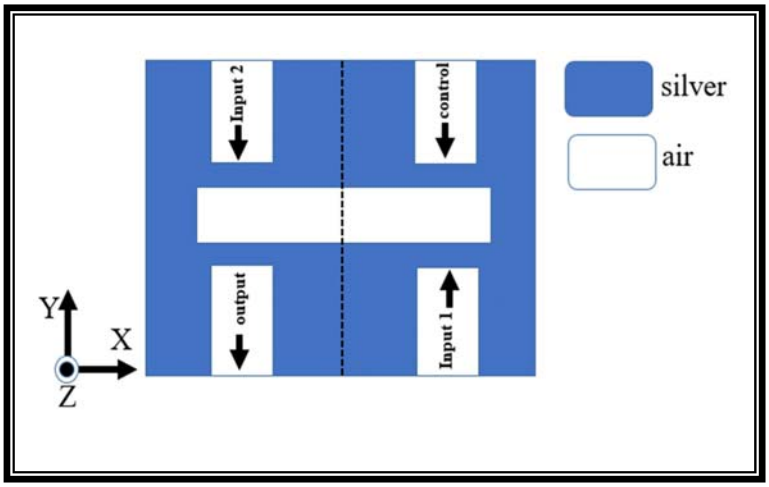


Figure 4.11 Structure for implementing an optical plasmonic AND logic gate

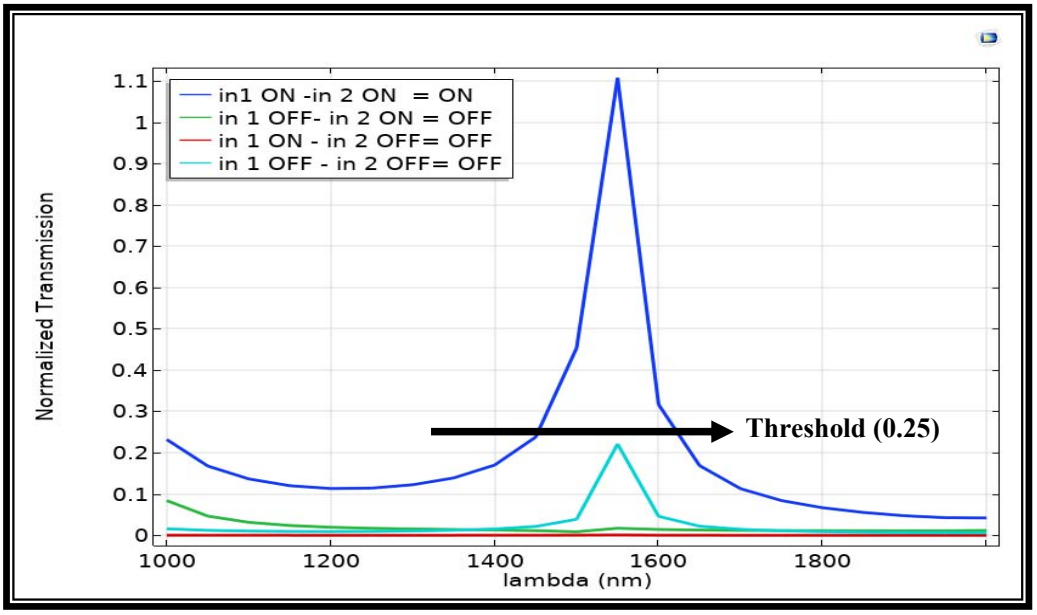


Figure 4.12 The spectrum of the transmissionshowing the correlation between the transmission and the wavelength for all states of the optical plasmonic AND logic gate

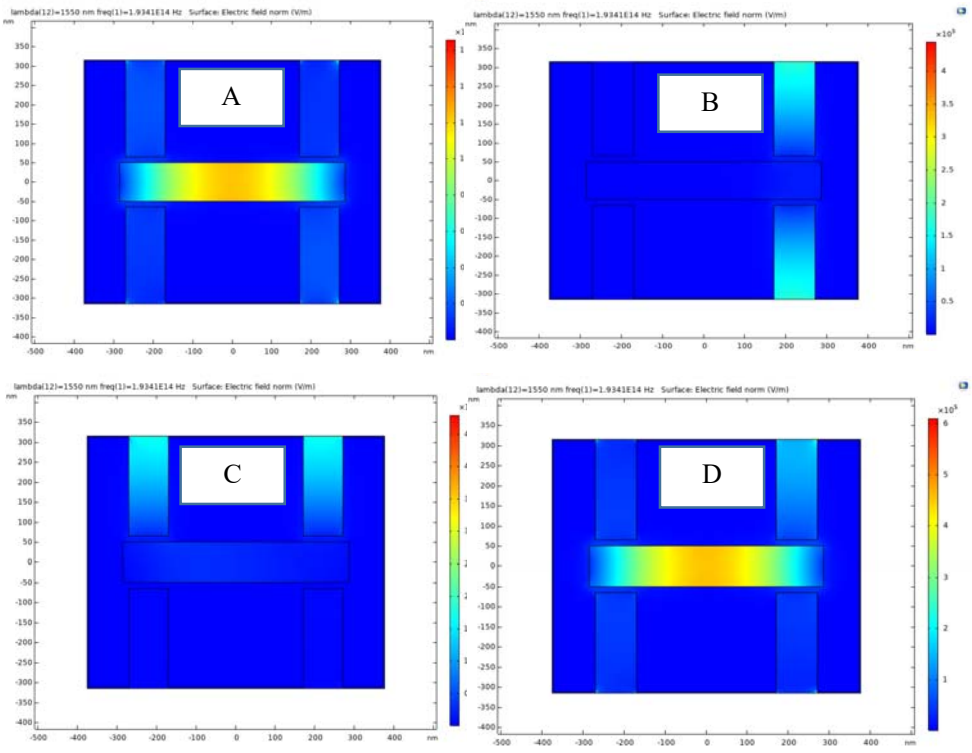


Figure 4.13 The electric field of states of AND gate in the structure (A) when the input in the first port is ON, (B) when the input in the second port is ON, (C) when the two inputs are ON, and (D) when the two inputs are OFF

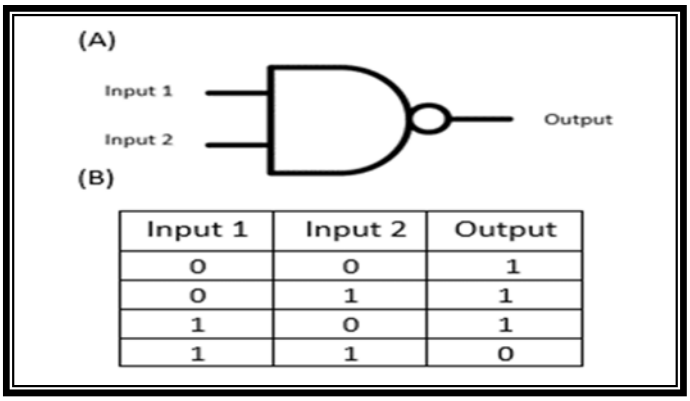
Table -4.3 Illustration the maximum transmission (T) and calculation of the maximum contrast ration for the plasmonic AND logic gate

Input optical power for single input port (P_{in}(w))	**1**	**1**	**1**	**1**
Output optical power for output port (P_{out} (w))	**1.107**	**0.017**	**0.0006**	**0.2209**
Inputs state	**on-on**	**off-off**	**on-off**	**off-on**
Output state	**on**	**off**	**off**	**off**
Minimum P_{out}|ON (W)	**1.107**			
Maximum P_{out}|OFF(W)	**0.2209**			
Maximum Contrast ratio (dB)	**7 (dB)**			
Maximum transmission (T)	**1.107**			

4.3.4 Optical Plasmonic NAND Logic Gate

To implement the NAND gate, the ports (2 and 4) will be considered as an input port, port (1) as a control port, always ON in all cases, and port (3) as an output port as shown in Figure 4.15. and the truth table of NAND gate and its shape shown in Figure 4.14, it can work as a NAND gate. Figure 4.16 shows the transmission of the NAND gate, with the highest transmission as 0.8%. When the first input port is ON in port (2), with the phase angle of the signal 0°, the output in port (3) will be ON and when the second input is ON in port (4) with the phase angle of the applied signal as 0° degrees, the output in port (3) will be ON. On the other hand, when the two inputs are OFF, the

output in port (3) will be ON, and when the two inputs are ON, the output in port (3) will be OFF, as shown in the Figure 4.16.



Input 1	Input 2	Output
0	0	1
0	1	1
1	0	1
1	1	0

Figure 4.14 (A) NAND logic gate symbol (B) NAND logic gate truth table

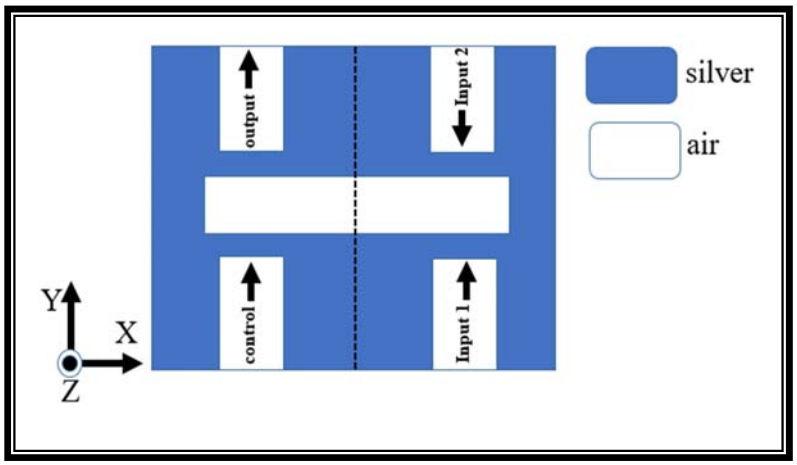


Figure 4.15 Structure for implementing an optical plasmonic NAND logic gate

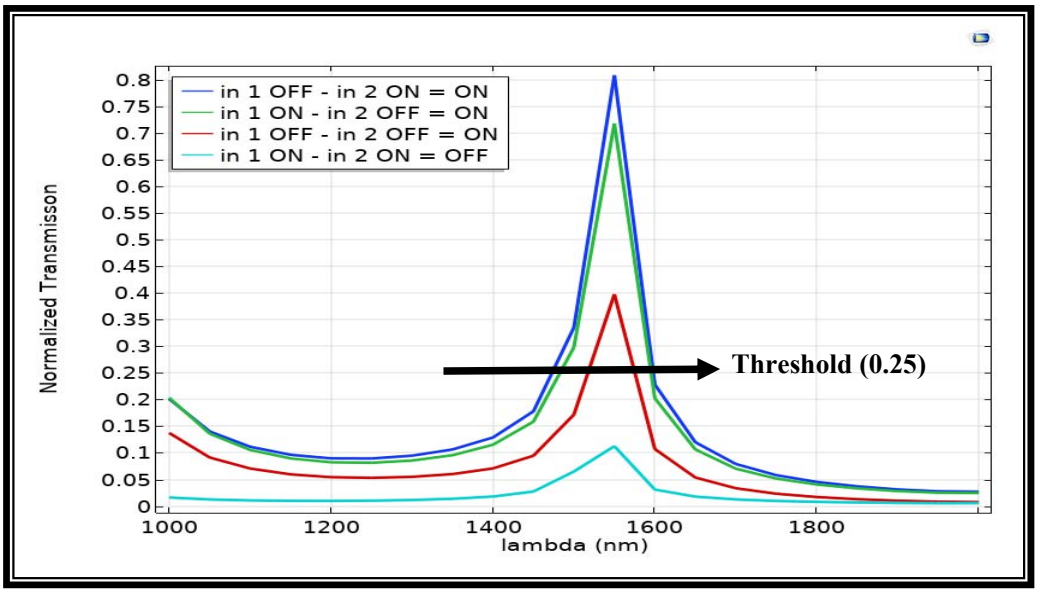


Figure 4.16 The spectrum of the transmission showing the correlation between the transmission and the wavelength for all states of the optical plasmonic NAND logic gate

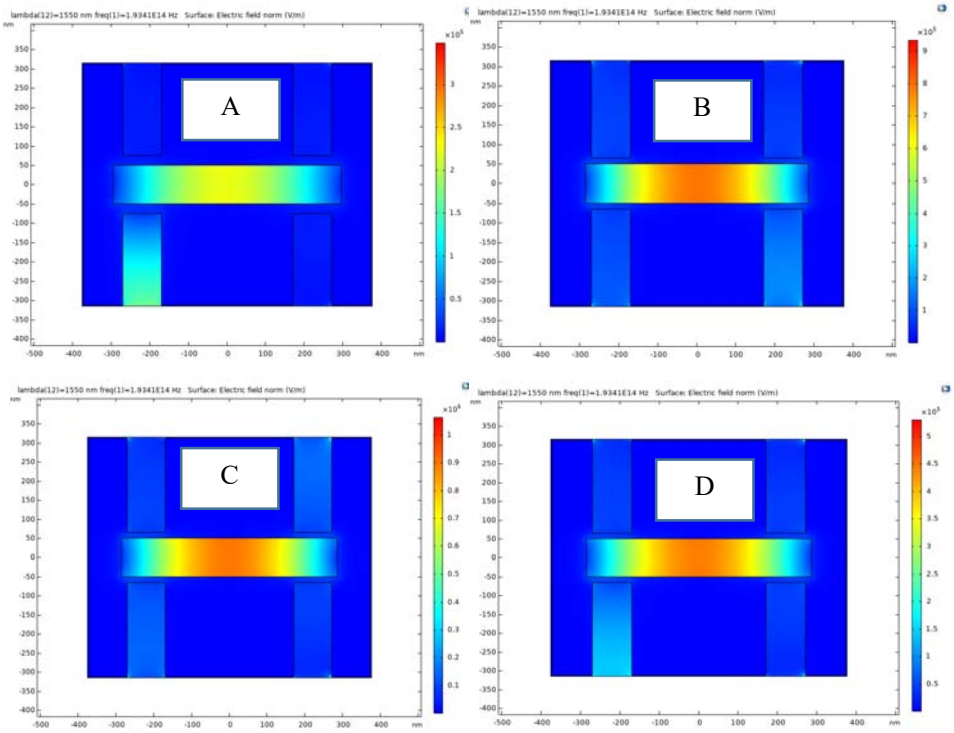


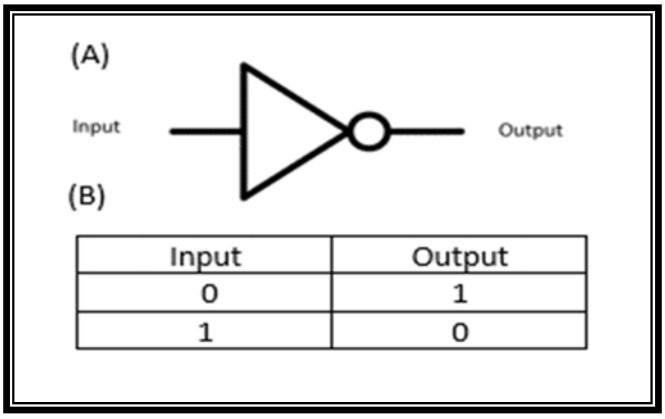
Figure 4.17 The electric field of states of NAND gate in the structure (A) when the input in the first port is ON, (B) when the input in the second port is ON, (C) when the two inputs are ON, and (D) when the two inputs are OFF

Table -4.4 Illustration the maximum transmission (T) and calculation of the maximum contrast ration for the plasmonic NAND logic gate

Input optical power for single input port (P_{in}(w))	**1**	**1**	**1**	**1**
Output optical power for output port (P_{out} (w))	**0.807**	**0.717**	**0.397**	**0.1125**
Inputs state	**off-on**	**on-off**	**off-off**	**on-on**
Output state	**on**	**on**	**on**	**off**
Minimum P_{out}|ON (W)	**0.397**			
Maximum P_{out}|OFF(W)	**0.1125**			
Maximum Contrast ratio (dB)	**5.4 (dB)**			
Maximum transmission (T)	**0.807**			

4.3.5 Optical Plasmonic NOT Logic Gate

To execute this gate, port (1) was considered as the input port, port (2) and port (3) was as control-1 port and control-2 port respectively. always in the ON state in all cases, port (4) as an output as shown in the Figure 4.19. As in the truth table of the NOT gate and its illustration in Figure 4.18, it can operate as a NOT gate. Figure 4.20 shows the transmission of the NOT gate, with the highest transmission obtained 0.8%. Hence, when port (1) is ON, the output in port (4) is OFF and when the input in port (1) is OFF, the output in port (4) is ON, as shown in the Figure 4.20.



Input	Output
0	1
1	0

Figure 4.18 (A) NOT logic gate symbol (B) NOT logic gate truth table

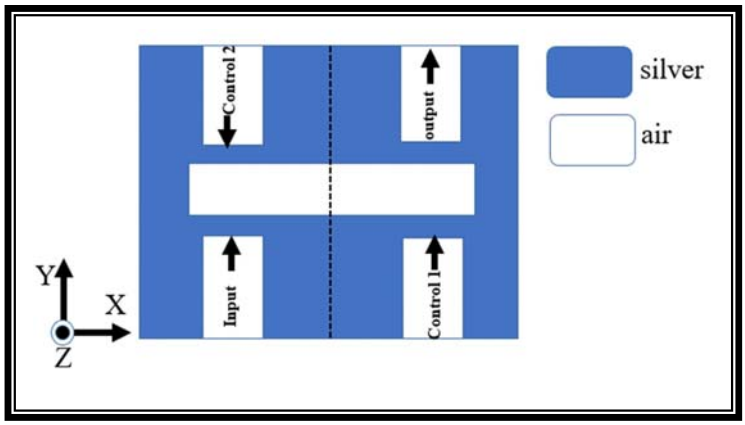


Figure 4.19 Structure for implementing an optical plasmonic NOT logic gate

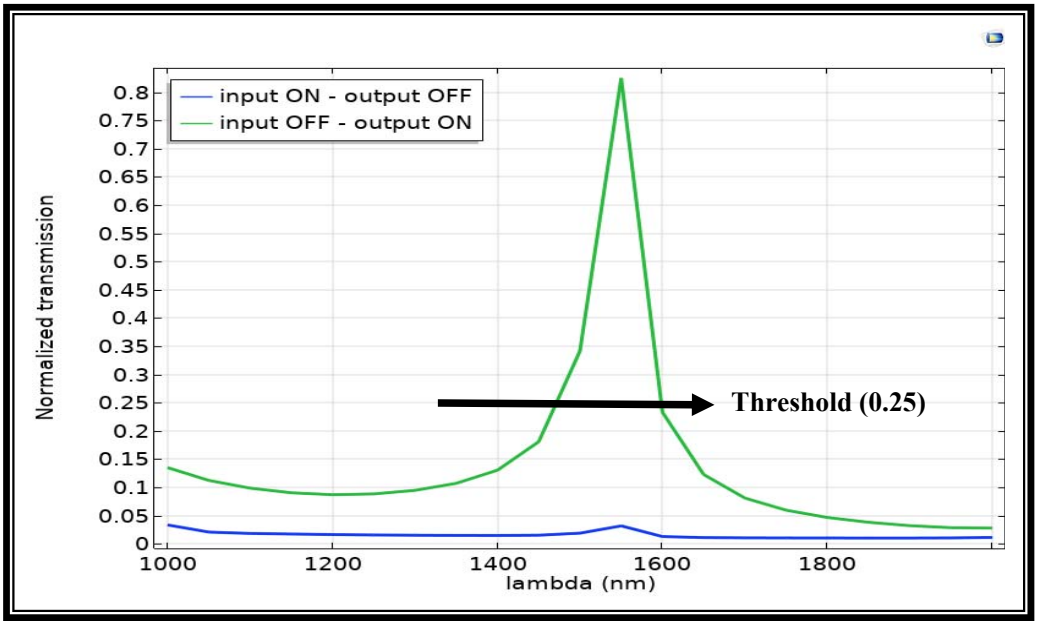


Figure 4.20 The spectrum of the transmission showing the correlation between the transmission and the wavelength for all states of the optical plasmonic NOT logic gate

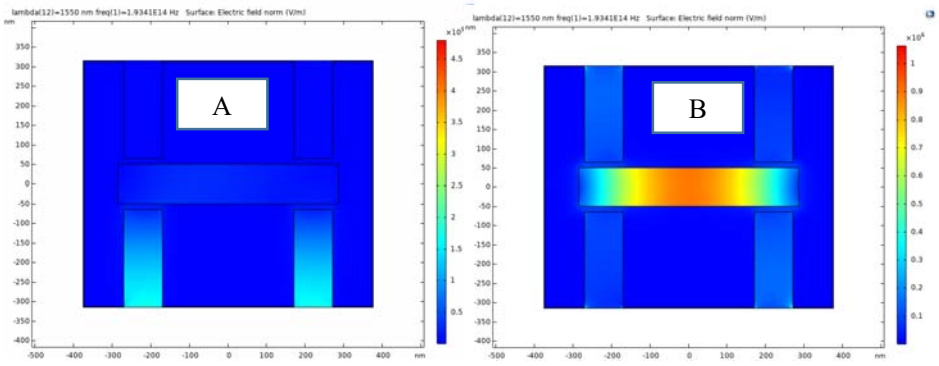


Figure 4.21 The electric field of states of NOT gate in the structure (A) when the input is ON, (B) when the input is OFF,

Table -4.5 Illustration the maximum transmission (T) and calculation of the maximum contrast ration for the plasmonic NOT logic gate

Input optical power for single input port (P_{in}(w))	**1**	**1**
Output optical power for output port (P_{out} (w))	**0.824**	**0.03**
Inputs state	**off**	**on**
Output state	**on**	**off**
Minimum P_{out}|ON (W)	**0.824**	
Maximum P_{out}|OFF(W)	**0.03**	
Maximum Contrast ratio (dB)	**14.3 (dB)**	
Maximum transmission (T)	**0.824**	

4.4 Summary

This chapter proves that the plasmonic technology is one of the best technologies adopted in minimizing the dimensions of optical devices which are used in communications. Five gates were designed: OR, NOR, AND, NAND and NOT gates in one structure with the same dimensions, the same wavelength and the same transmission threshold. The results were analyzed numerically using COMSOL MULTIPHSICES (5.5), where these gates were implemented depending on the optical interference feature between the propagated signals in the inputs and control port and the coupling process between the waveguides and the slot cavity. The results of simulations revealed that the dimension for this structure is (750× 650) nm and highest

transmission exceeded 100% in the OR and AND gate, reaching 121 % in OR gate and 110 % in AND gate, and the highest contrast ratio was in the OR and NOT gate, of more than (14 dB).

Chapter 5

Conclusion and Future Works

5.1 Summary and conclusions

Five optical plasmonic logic gates were implemented by COMSOL MULTIPHSICES (5.5) software, whose working principle is based on characteristics of the constructive and destructive interferences between the input and control ports. The transmission rate was controllable through parameters of the structure, such as the materials used in the construction of the structure, the refractive index of the selected materials, the locations of the ports for the control, input, and output signals, as well as the polarity of the signal directed at the control and input ports in both structures, but when installing all the parameters for one structure, the following was noticed:

1- The dimensions of the structure of the IMI PWs are much smaller than the structure using MIM waveguide due to the area of the metal used in building the structure, which is larger in the structure of MIM PWs because of the many free electrons in the metals that lead to fast dissipation of energy. This in turn shortens the propagation length in this type of waveguide, but the light confinement is stronger, as mentioned in the comparison between the waveguides in the second unit.

2- In the structure using IMI PWs, the transmission can be controlled by the distance between the waveguide and the nano-square-ring resonator. Hence, the best distance for best transmission is 7 nm. As for the structure using the MIM PWs, the transmission can be controlled by changing the distance between the waveguide and the nano-cavity slot where the best distance to obtain the highest transmission was 15 nm.

3- In the structure using the IMI PWs, the wavelength can be controlled by the outer rib length of the nano-square ring resonator as well as by the refractive index of the

insulating material used in synthesis of the structure. The best outer rib length of the nano-square ring resonator is 80 nm and the best refractive index of the insulating material is n = 1.424 to obtain the required wavelength of 1550 nm. Meanwhile, the structure using the MIM PWs, the wavelength could be controlled only by the width of the nano-slot cavity, where the best width was W_c= 560 nm to obtain the required wavelength of 1550 nm.

It is indicated that the structure using IMI PWs is better because it implements the five optical-plasma logic gates in this research with small dimensions of (350X300) nm. On the other hand, these gates are implemented in the second structure with an MIM PWs with larger dimensions of (750 X 650) nm as these dimensions are of great importance when using such structures in the synthesis of integrated photo-plasmonic circuits.

Table-5.1 Comparison between the structures and previous works

References	year		Maximum contrast ratio in (dB)	Maximum Transmission %	The performance measured	Size of the structure	Operating wavelength(s)	The logic gates implementation	Plasmonic waveguide(s)	
									IMI PWs	MIM PWs
Ref. [78]	In 2013			65.35 %	Maximum transmission	(2.4 X 3) µm	Only study	NOT		✓
Ref. [80]	In 2015			90%	Maximum transmission	(750X900) nm (1.5X1.8) nm	1535 nm	NOT,AND, and NOR		✓
Ref. [81]	In 2012		25 dB		Maximum Contrast ratio	(1220X1120) nm	525 nm	NAND,XOR ,and XNOR		✓
Ref. [82]	In 2018		13.9 dB		Maximum Contrast ratio	Complex system	Only study	OR, NOT, AND and EX-OR		✓
Ref. [83]	In 2019			84.06%	Maximum transmission	(2 X 3) µm	Only study	AND and NOR		✓
Ref.[85]	In 2019		12 dB		Maximum Contrast ratio	Complex system	Only study	OR and NOR		✓
Ref. [86]	In 2020		13.6 dB		Maximum Contrast ratio	Complex system	1310 nm	NOT	✓	
Proposed Work	In 2021	IMI	11.6 dB	124%	Maximum Contrast ratio And Maximum transmission	(300 X 350) nm	1550 nm	OR,NOR,AND, NAND and NOT	✓	✓
		MIM	14 dB	121%		(750 X 650) nm				

5.2 Future work

The following is plausible suggestions for prospective projects to be carried out.

1- To implementing the plasmonic gates experimentally through modern synthesis methods and devices.

2- To increasing the number of logic gates in the same single structure to be more compatible with the manufacture of integrated photo-plasmonic circuits, while minimizing the size of the structures to minimum size to be in line with their possible practical synthesis

3- To improve in the contrast ratio as much as possible for the plasmonic logic gates for better performance. And to Boost the transmission for all transmission states for all ON output states to 100% or more and Decreasing the transmission for all OFF output states to the lowest possible.

4- To synthesize a third structure using the plasmonic hybrid waveguide to implement the plasmonic logic gates and comparing the results between the three structures.

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List of Publications

1. Wissam abed jasim, Ali, Faris Mohammed, Ahmed Kareem Abdullah, and Mohammed Ahmed AbdulNabi. "Design and Simulation of Optical Logic Gates Based on (MIM) Plasmonic Waveguides and slot cavity resonator for Optical Communications." Journal of Physics: Conference Series. Vol. 1963. No. 1. IOP Publishing, (2021).
2. Jasim, Wissam Abed, et al. "Design and simulation of optical logic gates based on insulator-metal–insulator (IMI) plasmonic waveguides for optical communications." International Journal of Nonlinear Analysis and Applications 12.2 (2021): 2483-2497.

الخلاصة

بالرغم من ان الضوئيات تكون حلاً جيدا في زيادة سرعة نقل البيانات أفضل من الإلكترونيات بكثير الا ان تبقى هناك مشكلة وهي حدوث حالة التشتت التي تحدث في الإشارة عند تصغير حجم المكونات الضوئية لبناء الدوائر الضوئية المتكاملة .عندما جاءت تقنية البلازمونك (ادلة موجية بلازمية) بحل هذه المشكلة حيث يتم فيها حصر الموجات الكهرومغناطيسية بشكل جيد بين السطح المعدني -العازل او العازل -المعدني حيث هي كانت حلاً لمليء الفجوات الموجودة في الإلكترونيات (النطاق الترددي الواسع والسرعة العالية) وكذلك في الضوئيات (التغلب على حد التشتت الذي يحدث بسبب تصغير الحجم). حيث في هذه الرسالة يتم اقتراح تركيبين الأول باستخدام دليل موجي بلازمي عازل – معدن – عازل والثاني باستخدام دليل موجي بلازمي معدن – عازل – معدن. حيث تم اقتراح وتحليل وتصميم ومحاكاة وتنفيذ جميع البوابات الضوئية البلازمية باستخدام برنامج (COMSOL MULTIPHSECS 5.5) التركيب المقترح الأول يستخدم دليل موجي عازل - معدن - عازل (IMI) .اما التركيب الثاني المقترح يستخدم الدليل الموجي معدن -عازل - معدن (MIM). حيث ان البوابات المنطقية البلازمية التي تم تنفيذها في كل من التركيبين هي خمسة بوابات هي (NOT, OR , NOR, AND, NAND) حيث ان مبدا عمل هذه البوابات مبني على خاصية التداخلات البناءة والهدامة التي تحدث بين إشارات الادخال والتحكم حيث ان عتبة الارسال التي تم اختيارها هي 0.25% لكلا التركيبين لتنفيذ هذه البوابات الخمسة حيث يكون تنفيذ هذه البوابات بنفس التركيب ونفس الابعاد وبنفس الطول الموجي 1550 nm لجميع البوابات المنطقية البلازمية المقترحة في نفس التركيب الواحد. حيث تجاوز الارسال في بعض البوابات المنطقية البلازمية في كلا التركيبين 100% على سبيل المثال بوابة OR كان الارسال فيها هو 124% في التركيب الأول الذي يستخدم الدليل الموجي IMI. وكان الارسال في بوابة OR هو 121% في التركيب الثاني الذي يستخدم الدليل الموجي MIM حيث تم تنفيذ كل تركيب بمساحة صغيرة نسبيا حيث كانت nm (300X350) للتركيب الأول الذي يستخدم دليل موجي IMI وكانت المساحة nm (750X650) للتركيب الثاني الذي يستخدم دليل موجي MIM حيث تم ملاحظة من خلال نتائج المحاكات ان ابعاد التركيب تكون اقل عند استخدام دليل موجي نوع IMI .

تصميم ومحاكات بوابات منطقية ضوئية مبنية على ادلة موجية بلازمية مختلفة في الاتصالات الضوئية

الرسالة

مقدمة الى قسم هندسة تقنيات الاتصالات كجزء من متطلبات نيل درجة

الماجستير

تقدم بها

وسام عبد جاسم العذاري

إشراف

ا.م.د. احمد كريم عبد الله البكري

2021

جمهورية العراق

وزارة التعليم العالي والبحث العلمي

جامعة الفرات الاوسط التقنية

الكلية التقنية الهندسية- نجف

تصميم ومحاكات بوابات منطقية ضوئية مبنية على ادلة موجية بلازمية مختلفة في الاتصالات الضوئية

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