Counter and Time Delay

Lecture objectives: at the end of this lecture the student will able to:

1- Define the time delay.

2- Study the types of time delay.

3- Design all types of counters.

1- Time delay

1-1- **Definition of time delay:** number of instructions is written to delay in execution of microprocessor with certain interval. Time delay is designed by loading a certain register with a delay number and written some instructions and then DCR instruction to decrement the contents of time delay register by one and repeat this operation until this register equal to zero. Figure (4-1) below shown the flow chart to time delay.

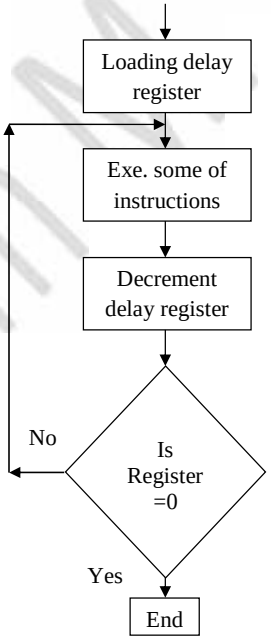


Figure (4-1) flowchart to time delay

1-2- Types of time delay: there are three types of time delay as shown below:

1-2-1- time delay using one register: in this type of time delay the register delay is one register loaded with 8-bit number in one loop as shown in program1below :

1-2-2- time delay using register pair: in this type of time delay the register delay is register pair loaded with 16-bit number in one loop as shown in program2 below:

1-2-3- time delay by loop with in loop: this time delay is used two loop one internal and other loop is external, these two loop can be designed by using one register or register pair as shown in program3 below:

Program 1

```
        MVI C,37 (delay reg.)
LOOP1   MVI A, 33
        RAR (some ins.)
        DCR C (decrement delay reg.)
        JNZ LOOP1 (condition)
        HLT
```

Program 2

```
        LXI B,234B (delay reg.)
LOOP1   MVI A, 33
        RAR (some ins.)
        DCX B (decrement delay reg.)
        MOV B,C
        ORA B
        JNZ LOOP1 (condition)
        HLT
```

Program 3

```
        MVI B,37 (delay reg. external loop)
LOOP 2  MVI D,FF (delay reg. internal loop)
LOOP1   MVI A, 33
        RAR (some ins.)
        DCR D (decrement delay reg. internal loop)
        JNZ LOOP1
        DCR B (decrement delay reg. external loop)
        JNZ LOOP2 (condition)
        HLT
```

1-3 Calculation of time delay: the interval of any program can be calculated by using the equation below:

$T_t = T_o + T_i$ ……4-1

Where T_t total time interval.

T_o time interval which required to execution the instructions out the loop.

T_i time interval which required to execution the instructions which in the loop.

$T_o = T_{state}\ (total) * t$

$T_i = T_{state}\ (total) * t * N_{10}$ ……4-3

Where N_{10} is the decimal equivalent to the number would loaded in delay register.

t is the processor time clock.

Example: Calculate the time delay to each program below: (let frequency is 1MHz)

Program 1

	MVI C,37 (delay reg.)	**$7T_{state}$**
LOOP1	**MVI A, 33**	**$7T_{state}$**
	RAR (some ins.)	**$4T_{state}$**
	DCR C (decr. delay reg.)	**$4T_{state}$**
	JNZ LOOP1 (condition)	**$10/7T_{state}$**
	HLT	**$6T_{state}$**

Program 2

	LXI B,234B (delay reg.)	**$10T_{state}$**
LOOP1	**MVI A, 33**	**$7T_{state}$**
	RAR (some ins.)	**$6T_{state}$**
	DCX B (decr. delay reg.)	**$4T_{state}$**
	MOV B,C	**$4T_{state}$**
	ORA B	**$4T_{state}$**
	JNZ LOOP1 (condition)	**$10/7T_{state}$**
	HLT	**$6T_{state}$**

Program 3

	MVI B,37 (delay reg. external loop)	**$7T_{state}$**
LOOP 2	**MVI D,FF (delay reg. internal loop)**	**$7T_{state}$**
LOOP1	***MVI A, 33***	**$7T_{state}$**
	RAR (some ins.)	**$6T_{state}$**
	DCR D (decr. delay reg. internal loop)	**$4T_{state}$**
	JNZ *LOOP1*	**$10/7T_{state}$**
	DCR B (decr. delay reg. external loop)	**$4T_{state}$**
	JNZ *LOOP2* (condition)	**$10/7T_{state}$**
	HLT	**$6T_{state}$**

Solution:

First $t=1/F=1/1*10^6 = 1\mu S$

For program 1

$T_t=T_o + T_i$

$T_o= [7T_{state\ (MVI\ C,37)} + 7T_{state\ (JNZ\ loop)} + 6T_{state\ (HLT)}]*t$

$=20\ T_{state}*1\ \mu S = 20\ \mu S$

$T_i=[7T_{state\ (MVI\ A,33)} + 4T_{state\ (RAR)} + 4T_{state\ (DCR\ C)} + 10T_{state\ (JNZ\ loop1)}]*t*55$

$=[25T_{state}]*t*55$

$=[25\ \mu S]*55=1375\ \mu S$

$T_t=20\ \mu S+1375\ \mu S=1395\ \mu S$

For program2

$T_o=[10T_{state\ (LXI\ B,234B)} + 7T_{state\ (JNZ\ loop)} + 6T_{state\ (HLT)}]$

$=23\ \mu S$

$T_i=[7T_{state\ (MVI\ A,33)} + 4T_{state\ (RAR)} + 4T_{state\ (DCX\ B)} + 4T_{state\ (MOV\ B,C)} + 4T_{state\ (ORA\ B)} + 10T_{state\ (JNZ\ loop1)}]*9035$

$=(33\ T_{state})*9035=(33\ \mu S)*9035=298155\ \mu S$

$T_t=23\ \mu S+298155\ \mu S=298178\ \mu S=298.178ms$

For program3

$T_o=[7T_{state\ (MVI\ C,37)} + 7T_{state\ (JNZ\ loop1)} + 6T_{state\ (HLT)}]$

$=20\ T_{state}=20\ \mu S$

$T_i=[7T_{state\ (MVI\ B,37)} + 7T_{state\ (MVI\ D,FF)} + \{7T_{state\ (MVI\ A,33)} + 4T_{state\ (RAR)} + 4T_{state\ (DCR\ D)} + \}*255 + 10T_{state\ (JNZ\ loop2)}*245 + 7T_{state\ (JNZ\ loop2)} + 4T_{state\ (DCR\ B)} +]*55 + 10T_{state\ (JNZ\ loop1)}*54$

Commented [DS1]: Internal loop

Commented [DS2]: External loop

$=[25\ T_{state} + \{3825\ T_{state}\} + 2450\ T_{state}]*55=[6300\ T_{state}]*55$

$=346500\ T_{state}=346500\ \mu S$

$T_t=T_o + T_i = 20\ \mu S+346500\ \mu S=346520\ \mu S=346.52ms$

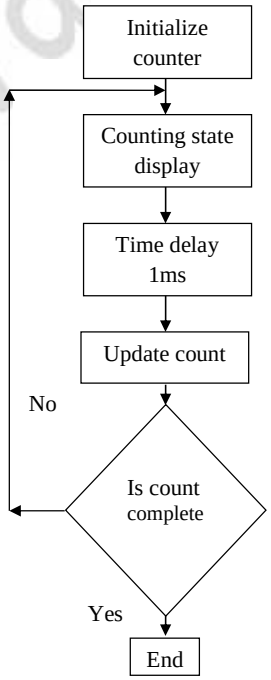
2- Counters:

2-1- Definition of counter: counter is a certain program can be executed in microprocessor to count number of counting states which these are necessary in some applications such as (traffic light, digital clock, control processes, and serial data transfer). All types of counters such as (up, down, Johnson, serial, parallel, decimal, etc.) can be executed by using 8085 microprocessor software with any time interval between counting states.

Example: write ALP (Assembly Language Program)to down counter mod(255) and display the counting states in output port with time delay (1ms) for each counting state. Let the processor operate with frequency 2MHz.

Solution: below flowchart to this program

	MVI A,FF	**7T$_{state}$**
A1:	**OUT 02**	**10T$_{state}$**
	MVI D, XX	**7T$_{state}$**
A2:	**DCR D**	**4T$_{state}$**
	JNZ A2(delay)	**10/7T$_{state}$**
	DCR A	**4T$_{state}$**
	JNZ A1(Count display)	**10/7T$_{state}$**
	HLT	**6T$_{state}$**



Now, must loading register **D** with certain number to getting the time delay 1ms, this number calculated as below:

First $t=1/F=1/2*10^6 = 0.5\mu S$

$T_t=T_o + T_i$

Where $T_t=1ms$

$T_o=[7T_{state\ (MVI\ A,FF)} + 10T_{state\ (OUT\ 02)} + 7T_{state\ (MVI\ DXX)} + 7T_{state\ (JNZ\ A2)} + 4T_{state\ (DCR\ A)} + 10T_{state\ (JNZ\ A1)}] * 0.5\mu S$

$=[45\ T_{state}] * 0.5\mu S=22.5\ \mu S$

$T_i=[(4T_{state\ (DCR\ D)} * N_{10})+ (10T_{state\ (JNZ\ A2)} * (N_{10}-1))]*0.5\ \mu S$

$=(2* N_{10})+5* (N_{10}-1)$

$=(7\ N_{10}-5)\ \mu S$

By return to initial equation

$T_t=T_o + T_i$

$1000\ \mu S=22.5\ \mu S+ (7\ N_{10}-5)\ \mu S$

$1000\ \mu S=22.5\ \mu S+7\ N_{10}\ \mu S-5\ \mu S$

$1000\ \mu S=17.5\ \mu S+7\ N_{10}\ \mu S$

$N_{10}=1000-17.5/7=140.34=140$

Therefore must loading equivalent to 140 in hexadecimal which equal (8C) in register **D.**

Home work:

1- Calculate the required time to execute the JPE instruction if the condition is satisfying. Let the processor operate with 4 MHz frequency.

2- write ALP operate as up/down counter mod(32) with time delay 2ms between each two counting states.