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8085 Microprocessor

Lecture 3

المدرس ضرغام الخفاف الاسدي

Third Year lecture notes

Avionics Engineering Dept.

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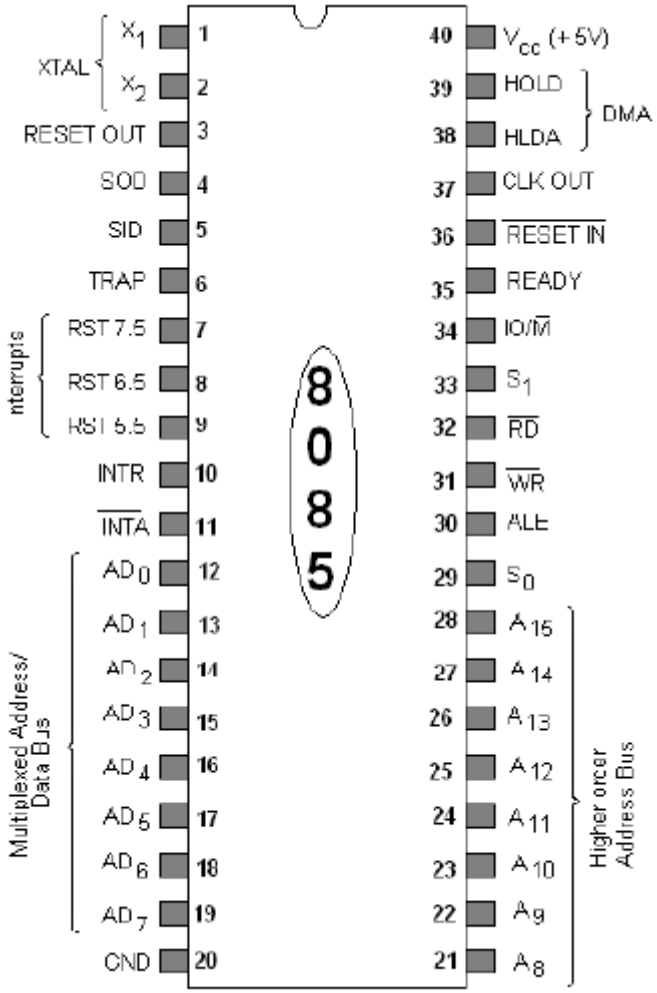
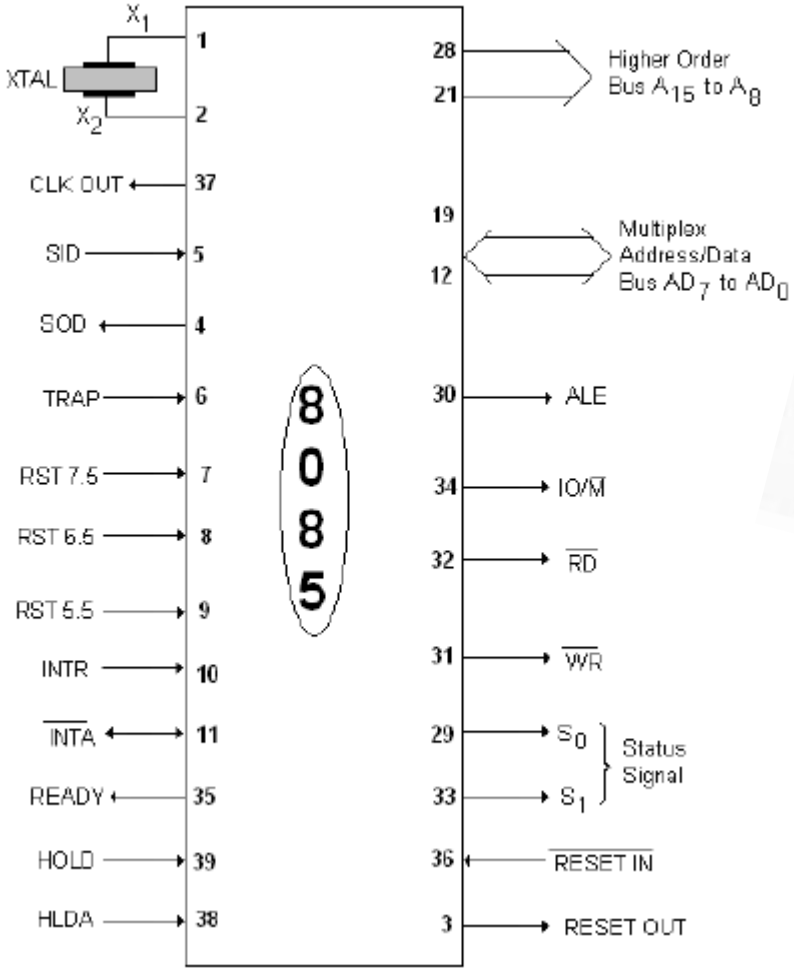
8085 Microprocessor Proprieties

- Number of transistors 6200.
- Dimension is (164*222 mm)
- 40 pin in dual-in-line package as shown in fig.
- Clock frequency is 3.125 MHz with supply of +5V.

Pin description of 8085





Pin No. 1&2 (X1, X2): Two pins X1 and X2 are provided to be externally connected to a quartz crystal. The clock signal of fixed frequency is generated through the internal circuitry of the processor. The frequency at which the microprocessor 8085 works is half of the crystal frequency. The quartz crystal of 6.144 MHz is used in this processor. This gives the clock frequency of 3.072 MHz (half of the crystal frequency) of 50% duty cycle. The clock period is of about 320 nsec. The output of the clock frequency is also available at CLK out terminal.

PIN NO. 3 It is active high signal used to reset the peripherals connecting with microprocessor system where this signal is supplied by 8085 microprocessor . When reset signal become low, the proceeding starting in operating.

PIN NOS. 4 and 5 indicate SOD (Serial Out Data) and SID (Serial In Data) terminals respectively. These pins are associated with Serial Input/Output control unit for 8085 microprocessor. As already discussed these pins are used for the serial data transmission. The SOD output pin can deliver a serial data stream to a peripheral device.

PIN NOS. 6 to 11 The interrupt control unit of the microprocessor contains these pins. The Pins 6 to 11 are restart interrupts named as in table below: The TRAP has the highest priority and INTR has the lowest priority. The priority level is of importance if two or more interrupts become active at the same time. The TRAP is non-maskable interrupt. It is both edge and level sensitive. The interrupts (TRAP, RST 7.5, RST 6.5 and RST 5.5) are also called vector interrupts, as each interrupt has fixed memory location (vector location) for the transfer of control from the normal execution of the routine. The vector locations of these interrupts are given in table 5.4. As soon as any of these pins 6 to 10 are active (high), the internal circuit of 8085 stops the normal execution of program and the program control is transferred to the corresponding memory location (vector location).

Interrupts	Priority
TRAP	1
RST 7.5	2
RST 6.5	3
RST 5.5	4
INTR	5

Interrupts	Memory locations
TRAP	0024 H
RST 7.5	003C H
RST 6.5	0034 H
RST 5.5	002C H

INTR (Pin No. 10) is a general purpose interrupt and has the lowest priority. As soon as Pin No. 10 is high, the microprocessor stops the execution of normal program and after completing the instruction at hand, it goes to CALL instruction. The INTR is enabled or disabled by the instructions ET (Enable Interrupts) or DI (Disable Interrupts) respectively.

The Pin No. 11 is an Interrupt Acknowledge (INTA) signal. A low (logic 0) to this pin indicate that the microprocessor has acknowledged the request from the peripheral device. It is also used to activate the interrupt controller.

PIN NOS. 12 to 19 (AD0-AD7) form bi-directional multiplexed Address/Data Bus. The least significant 8 bits of the memory address (or I/O Address) appear on the bus during the first T-states of a machine cycle. It then becomes the data bus during the next T-states.

PIN NO. 20 is the ground terminal.

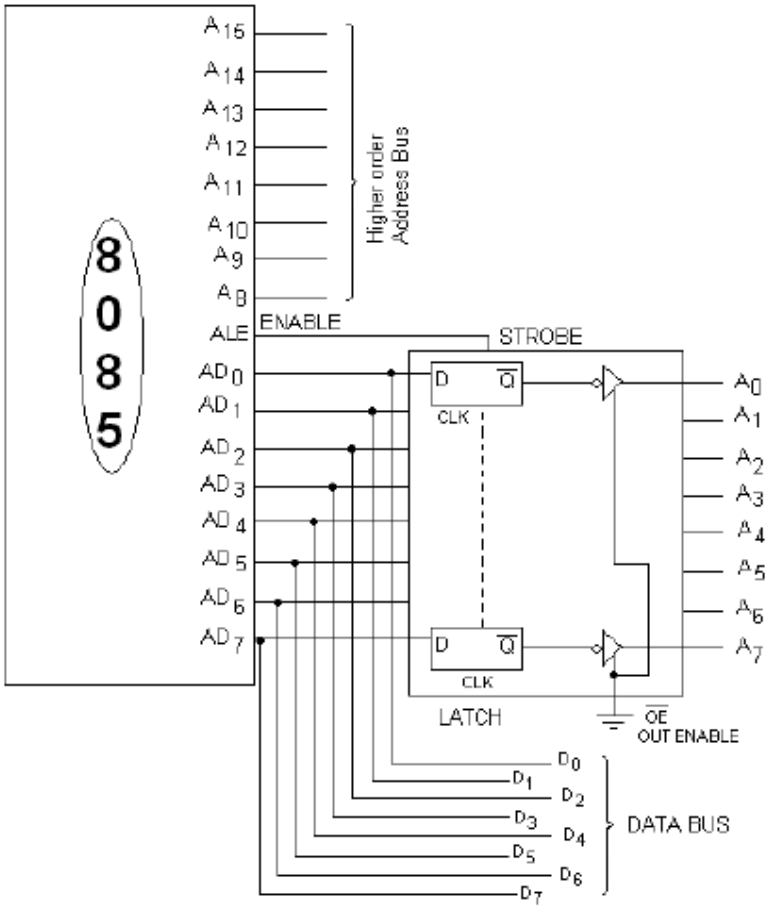
PIN NOS. 21 to 28 (A8-A15) form unidirectional most significant 8 bits of memory address or 8 bits of the I/O address.

PIN NOS. 29 to 33 labled as S0 and S1 respectively are known as status signals. These status signals along with IO/M signal indicate the various operations as indicated in table

.

Machine cycle	IO/$\overline{M}$	Status S_1	Status S_0	Control signals
Op code Fetch	0	1	1	$\overline{RD} = 0$
Memory Read	0	1	0	$\overline{RD} = 0$
Memory Write	0	0	1	$\overline{WR} = 0$
I/O Read	1	1	0	$\overline{RD} = 0$
I/O Write	1	0	1	$\overline{WR} = 0$
Interrupt Ack.	1	1	1	$\overline{INTA} = 0$
HALT	HI-Z	0	0	
HOLD	HI-Z	X	X	$\overline{RD}, \overline{WR} = Z$
RESET	HI-Z	X	X	$\overline{INTA} = 1$

The Pin No. 30 is known as ALE (Address Latch Enable) terminal. When this signal is high the information carried on the multiplexed address/data bus (AD0-AD7) is the lower 8 bits of the address. It also enables the low order address (AD0-AD7) from the multiplexed address/data bus to latch either into the memory or the external latch. The ALE signal separates the low order address and data from the multiplexed address/data Bus.



PIN NOS. 31, 32 and 34 The Pin Nos. 31 and 32 are the two control signals WR (Write bar) and RD (Read bar) respectively. The pin 34 carries IO/M signal which is one of the status signals. The other status signals are S0 and S1 discussed earlier. A low WR signal generated by the microprocessor sends (writes) data into I/O devices or memory. Similarly, a low RD signal generated by the microprocessor reads (receives) the data from the I/O devices or memory locations. The IO/M signal indicates whether the address on the address bus is meant for I/O devices. However, a low to this signal indicates that the address on the address bus is meant for memory location. The RD ,WR and IO/M signals function together.

PIN NO. 35 is known as READY signal which forces the microprocessor to wait till the data become available from the memory or input/output devices. This signal is needed to synchronize the speed of the microprocessor with I/O devices or memory as the memory or I/O devices are not as fast as the microprocessor. When the READ signal is low, the microprocessor waits till the READY signal is 1. As soon as READY signal is 1, the microprocessor knows that the data are available from the memory or I/O devices.

PIN NO. 36 This pin is signal. This input carrying signal may be operated by the operator using the RESET IN button provided externally or it may be operated directly from the other source. When this signal is low (momentarily), the CPU will reset the program counter, instruction register, all interrupts (except TRAP) are disabled, SOD signal becomes low and Data, address and control buses are floated. When this signal goes high, the data processing begins.

PIN NO. 37 This pin carries CLK OUT signal. It is derived from the on-chip oscillator, which goes to peripherals to synchronize their timings.

PIN NOS. 38-39 are the HOLD and HLDA (Hold Acknowledge) signals respectively. These signals are used in DMA (Direct Memory Access) operations. As shown in figure 5.7, when any I/O device indicates that the data are ready for DMA transfer, a high HOLD signal is sent by the DMA controller to the 8085 microprocessor. It is in fact a request signal from the DMA controller to the microprocessor. The microprocessor then sends a high signal to DMA controller indicating that the microprocessor has received the request from the I/O devices and will relinquish the address, data and control bus after completing the current instruction. The DMA controller thus carries out the data transfer. A low HOLD signal will return the control to the microprocessor.

PIN NO. 40 The pin 40 is +VCC, which is to be externally connected to +5 volt d.c. supply.

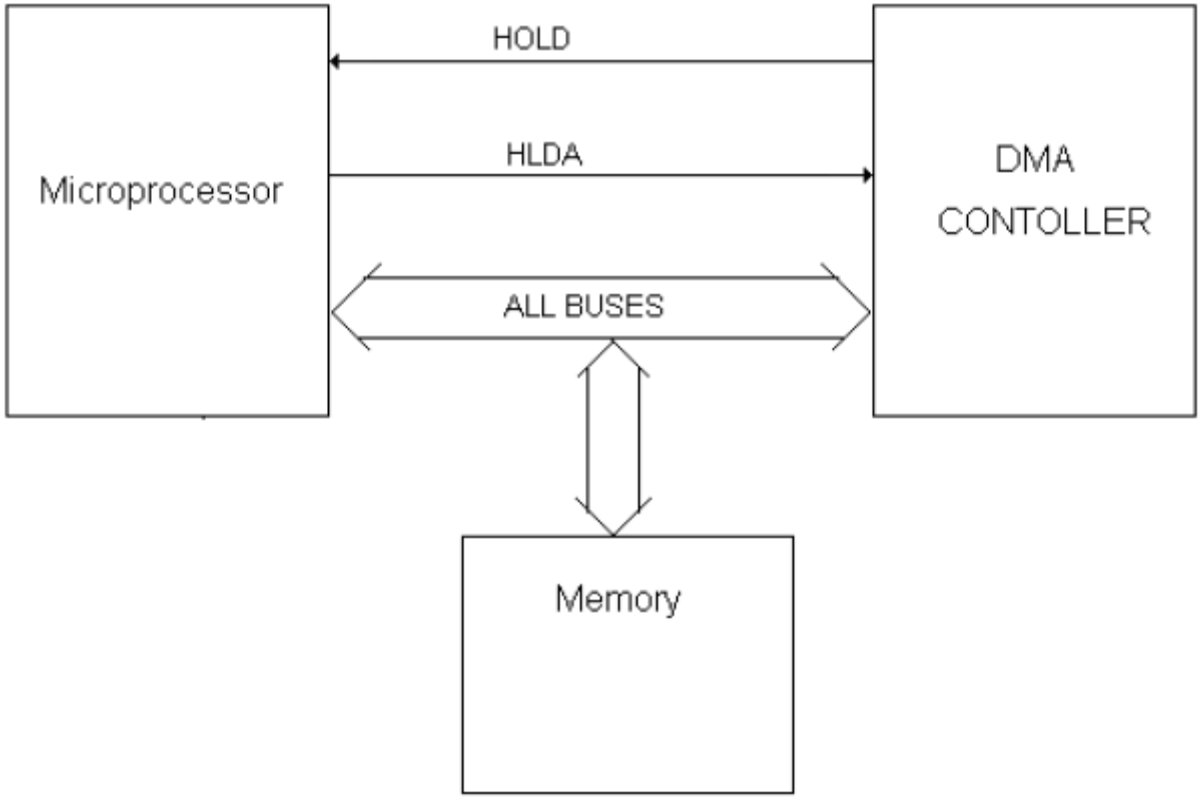


Fig. 5.7

Thank you